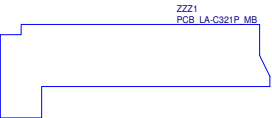


MODEL NAME : *Bold_Peak_II (AAE00)*
PCB NO : *LA-C321P (DAA000A6000)*
BOM P/N :

Dell/Compal Confidential

Schematic Document

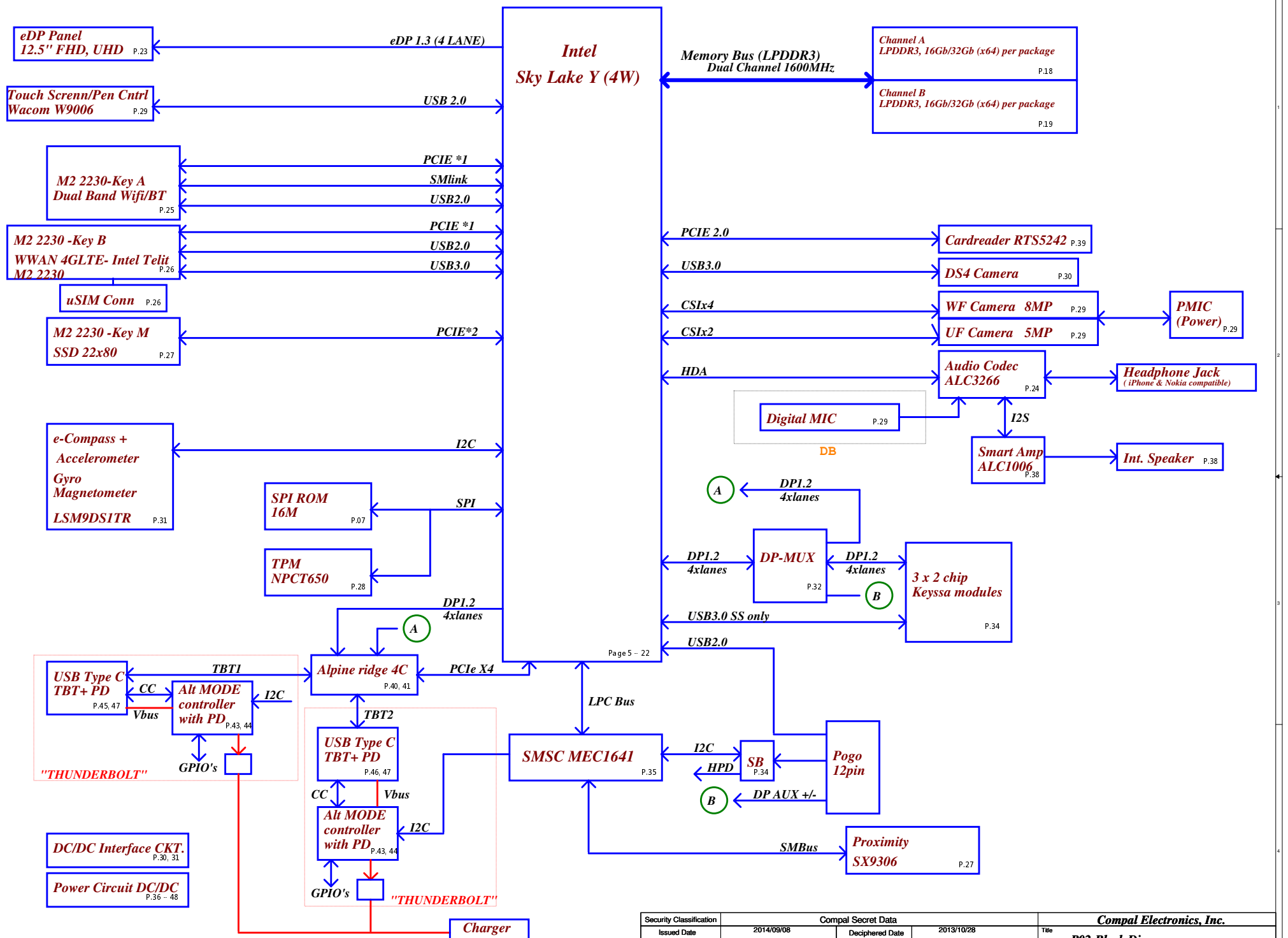
Bold Peak2 (Skylake Y)

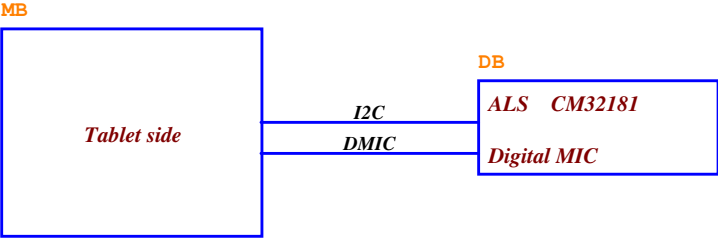


2015-07-03

Rev: 0.7 (X06)

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				Date: Wednesday, July 08, 2015	Rev 0.7(X06)
				Sheet	1 of 61





Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	
0	240K +/- 5%	4700p	0.1, 0.2	Pre-EVT1, 2
1	130K +/- 5%	4700p	0.3	EVT
2	62K +/- 5%	4700p	0.4	DVT1
3	33K +/- 5%	4700p	0.5	DVT2
4	8.2K +/- 5%	4700p	1.0	PVT
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	NC			

SMBUS Control Table

	SOURCE	Base	BATT	Charger	TBT	XDP	SB
PCH_SML0CLK PCH_SML0DATA	PCH						
PCH_SML1CLK PCH_SML1DATA	PCH						
MEM_SMBCLK MEM_SMBDATA	PCH					V	V
EC_SMB00_CLK EC_SMB00_DAT	MEC1641						
EC_SMB01_CLK EC_SMB01_DAT	MEC1641				V		
EC_SMB03_CLK EC_SMB03_DAT	MEC1641		V				
EC_SMB04_CLK EC_SMB04_DAT	MEC1641			V			
EC_SMB05_CLK EC_SMB05_DAT	MEC1641	V					

Link

USB 3.0 PORT#	DESTINATION
1	Debug
2	WWAN
3	DS4 camera
4	Keyssa

USB 2.0 PORT#	DESTINATION
1	BASE
5	WWAN
7	Touch
3	BT
9	Debug

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	B	DP MUX
	C	TBT
	D	

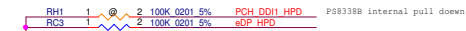
PCI EXPRESS	DESTINATION
Lane 1	TBT (Alpine Ridge, Gen3)
Lane 2	TBT (Alpine Ridge, Gen3)
Lane 3	TBT (Alpine Ridge, Gen3)
Lane 4	TBT (Alpine Ridge, Gen3)
Lane 5	WWAN (NGFF, Gen3)
Lane 6	
Lane 7/ SATA0	SSD (NGFF, Gen3)
Lane 8	SSD (NGFF, Gen3)
Lane 9	WLAN (NGFF, Gen2)
Lane 10	Cardreader (Gen2)

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE1	TBT
	CLKOUT_PCIE2	Cardreader
	CLKOUT_PCIE3	NGFF SSD
	CLKOUT_PCIE4	NGFF (WLAN)
	CLKOUT_PCIE5	NGFF (WWAN)

FLEX CLOCKS	DESTINATION
CLKOUT_LPC_0	EC LPC
CLKOUT_LPC_1	Debug

Symbol Note :

- @ : means de-pop
-  : means Digital Ground
-  : means Analog Ground



Functional Strap Definitions

GPP_E19 (Internal Pull Down): DDPB_CTRLDATA

0 = Port B is not detected.

1 = Port B is detected.

GPP E21 (Internal Pull Down): DDPC CTRLDATA

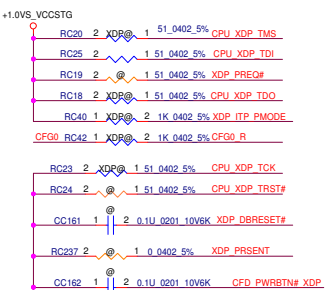
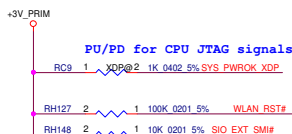
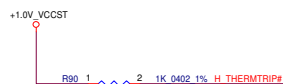
0 = Port C is not detected.

1 = Port C is detected.

GPP E23 (Internal Pull Down): DDPD_CTRLDATA

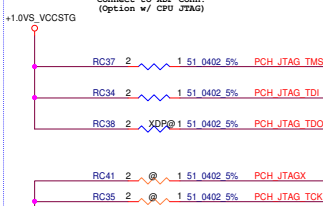
0 = Port D is not detected.

1 = Port D is detected.



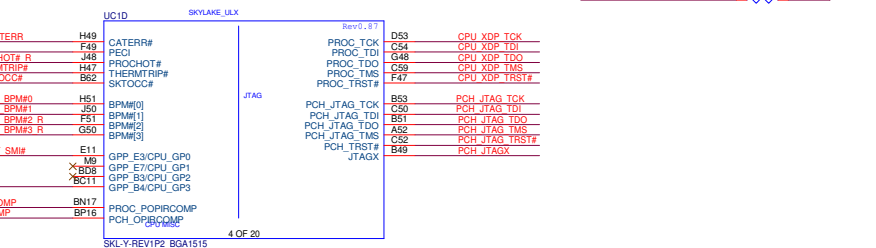
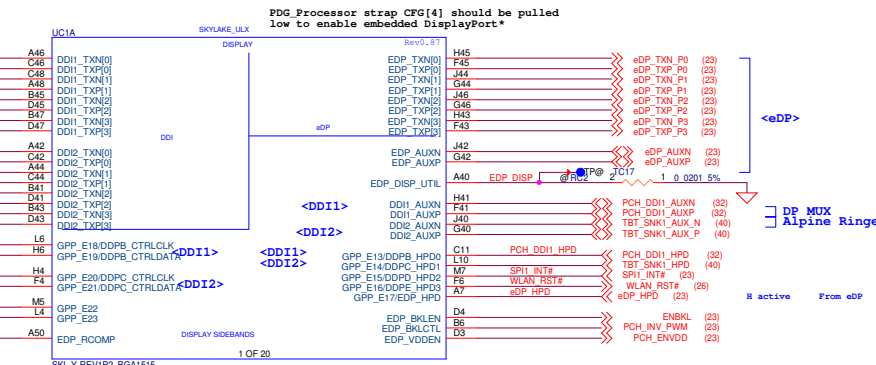
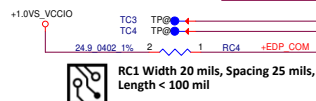
PU/PD for PCH JTAG signals

Connect to XDP Conn.
(Option w/ CPU JTAG)

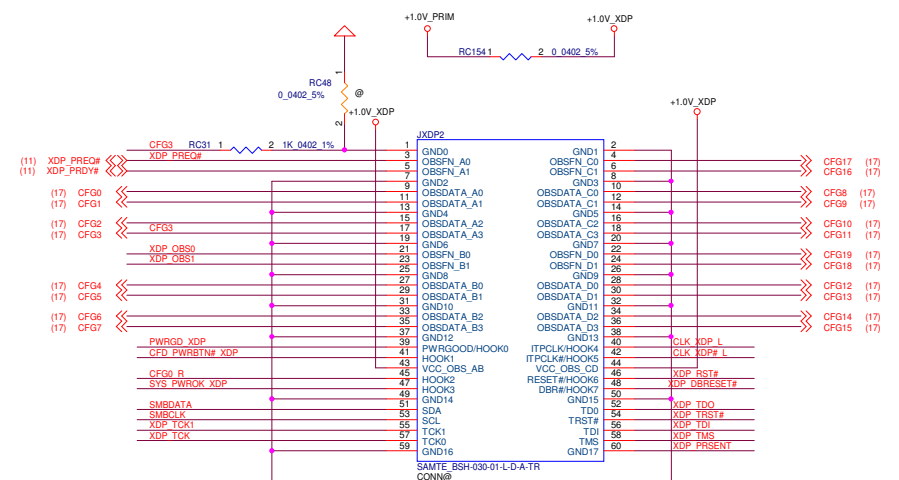


DP MUX

Alpine Ridge



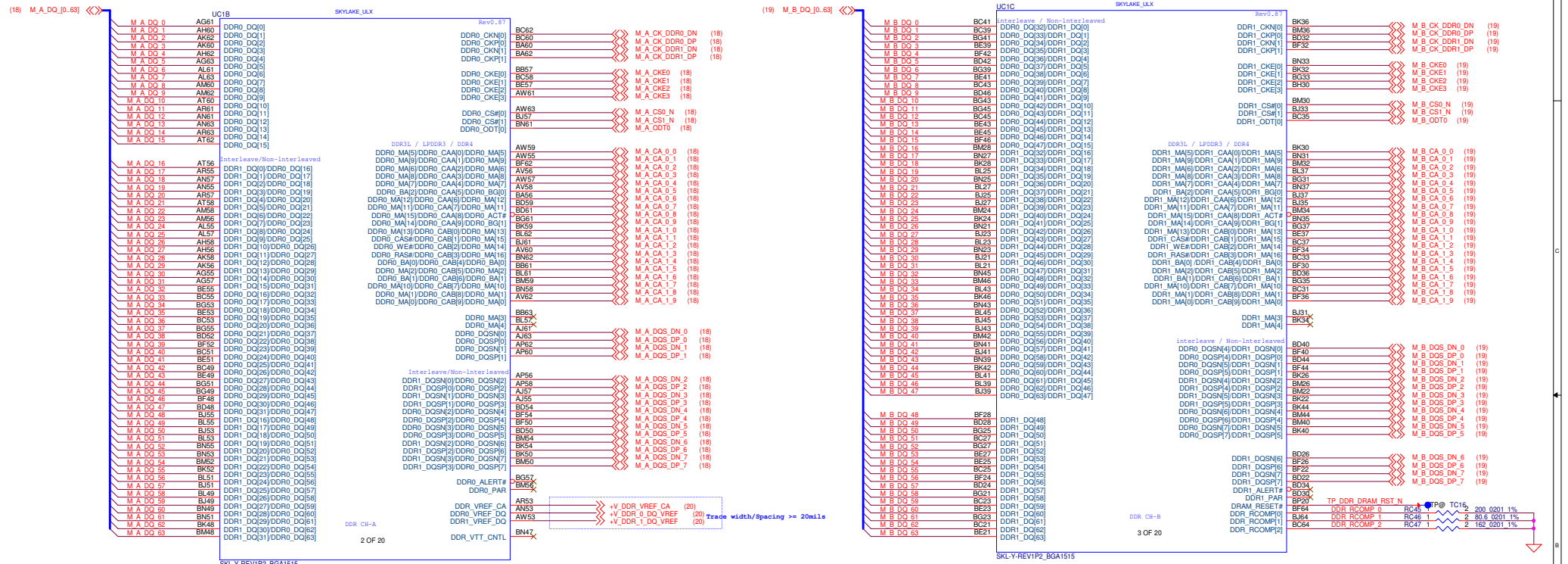
XDP CONN



footprint "SAMTE_BSH-030-01-L-D-A-TR_60P-S"
non-location fear

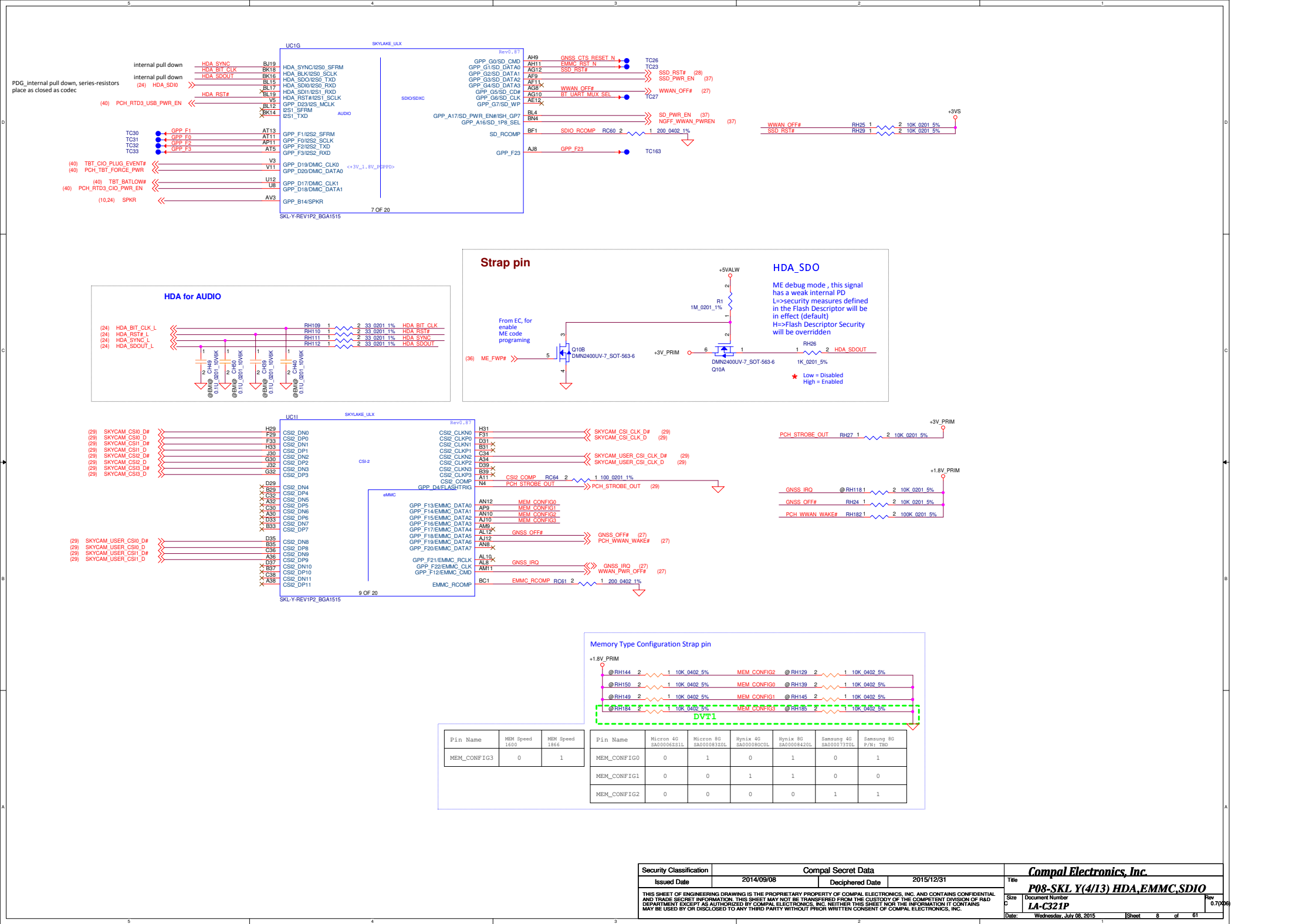
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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					LA-C321P	07000
				Date:	Wednesday, July 08, 2015	Sheet 5 of 61

Non-interleaved Memory

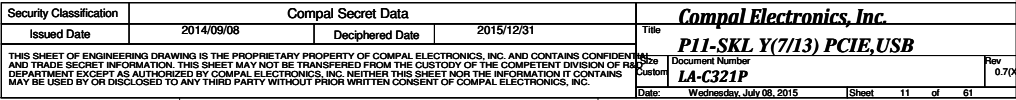


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				Size	Document Number	Rev
				C	LA-C321P	0.7006
Date: Wednesday, July 08, 2015				Sheet	6	of 61









VCCST : Sustain voltage for processor standby modes
VCCSTG : Gated sustain voltage for processor standby modes

VDDQC trace
filter width = 6mm
Total etch length
= 186.94mils
PDG P597

CC3
0.1U_0201_10V6K

+VDDQ_CPU_CLK

RH61
0.0402_5%

+1.0V_VCCST

+1.0VS_VCCSTG

+1.2V_VCCSFR_OC

+1.0V_VCCSFR

V26

R26

AE27

R27

T27

+1.0V_VCCST

RC106 1

2 0.0402_5%

+1.0V_VCCSFR

CC17

0.1U_0201_10V6K

+1.2V_VCCSFR_OC

RC102 1

2 0.0402_5%

+VDDQ_CPU_CLK

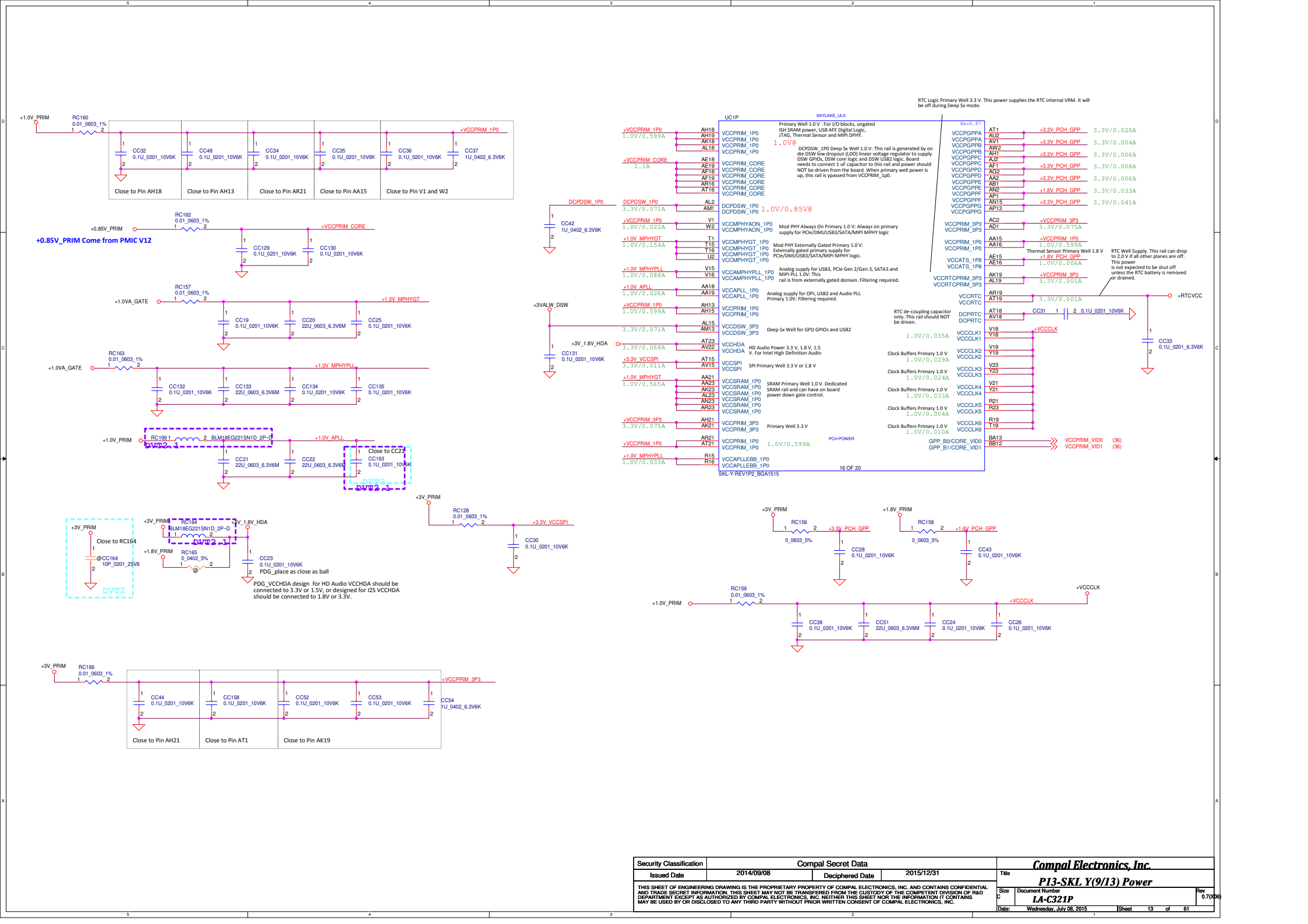
CC15

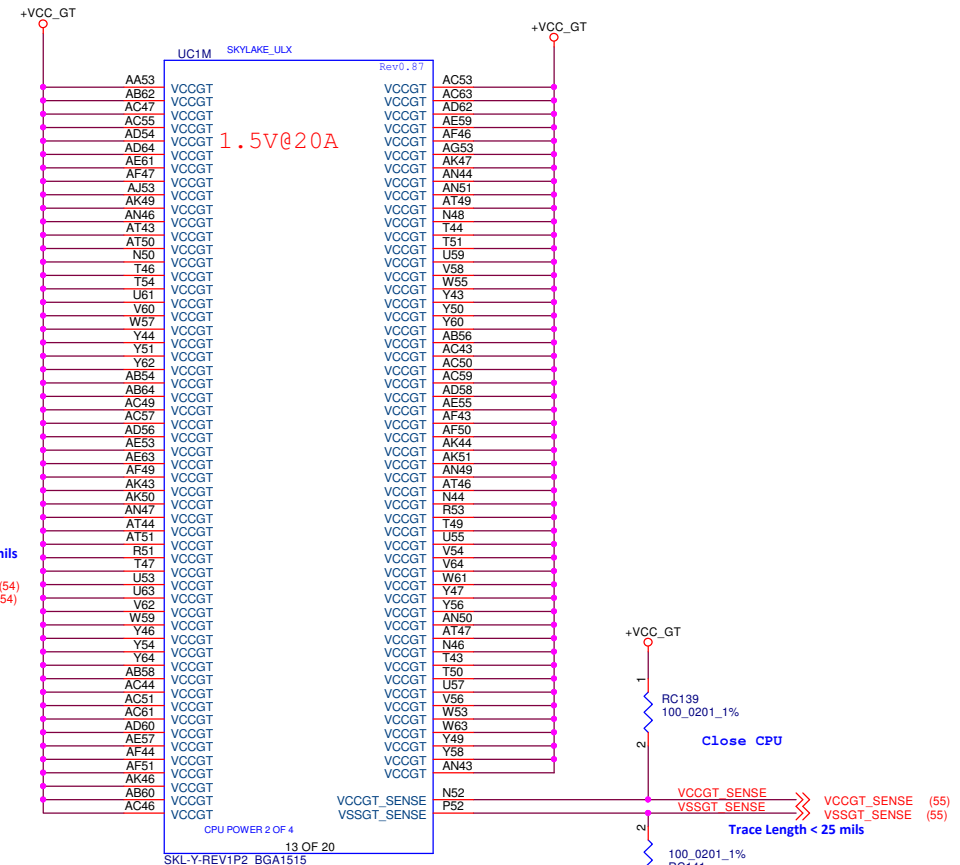
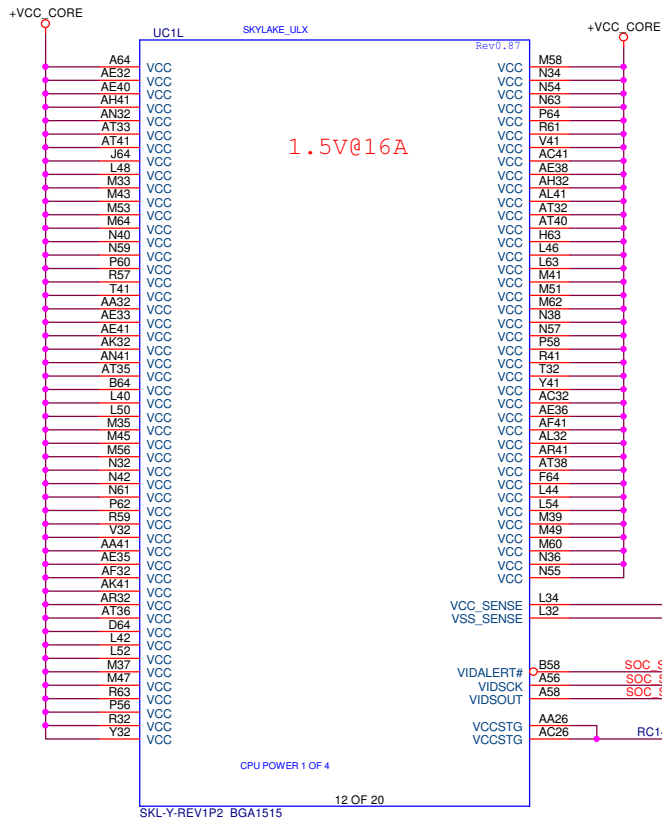
0.1U_0201_10V6K

+1.0VS_VCCSTG

CC18

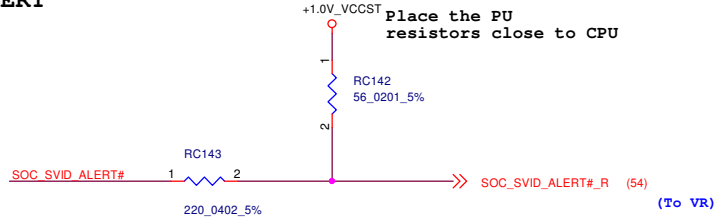
0.1U_0201_10V6K





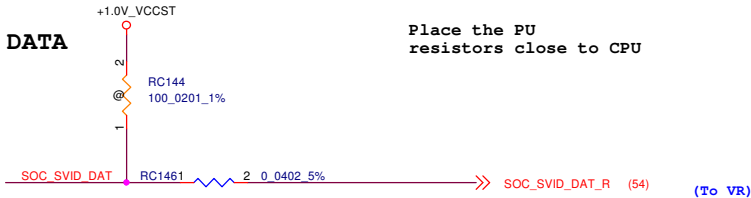
SVID ALERT

Place the PU resistors close to CPU



SVID DATA

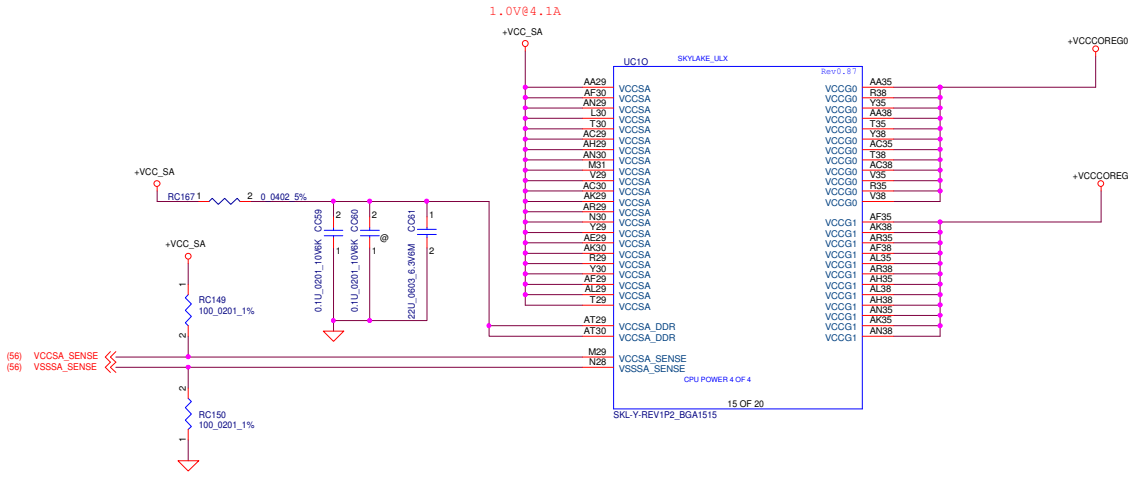
Place the PU resistors close to CPU

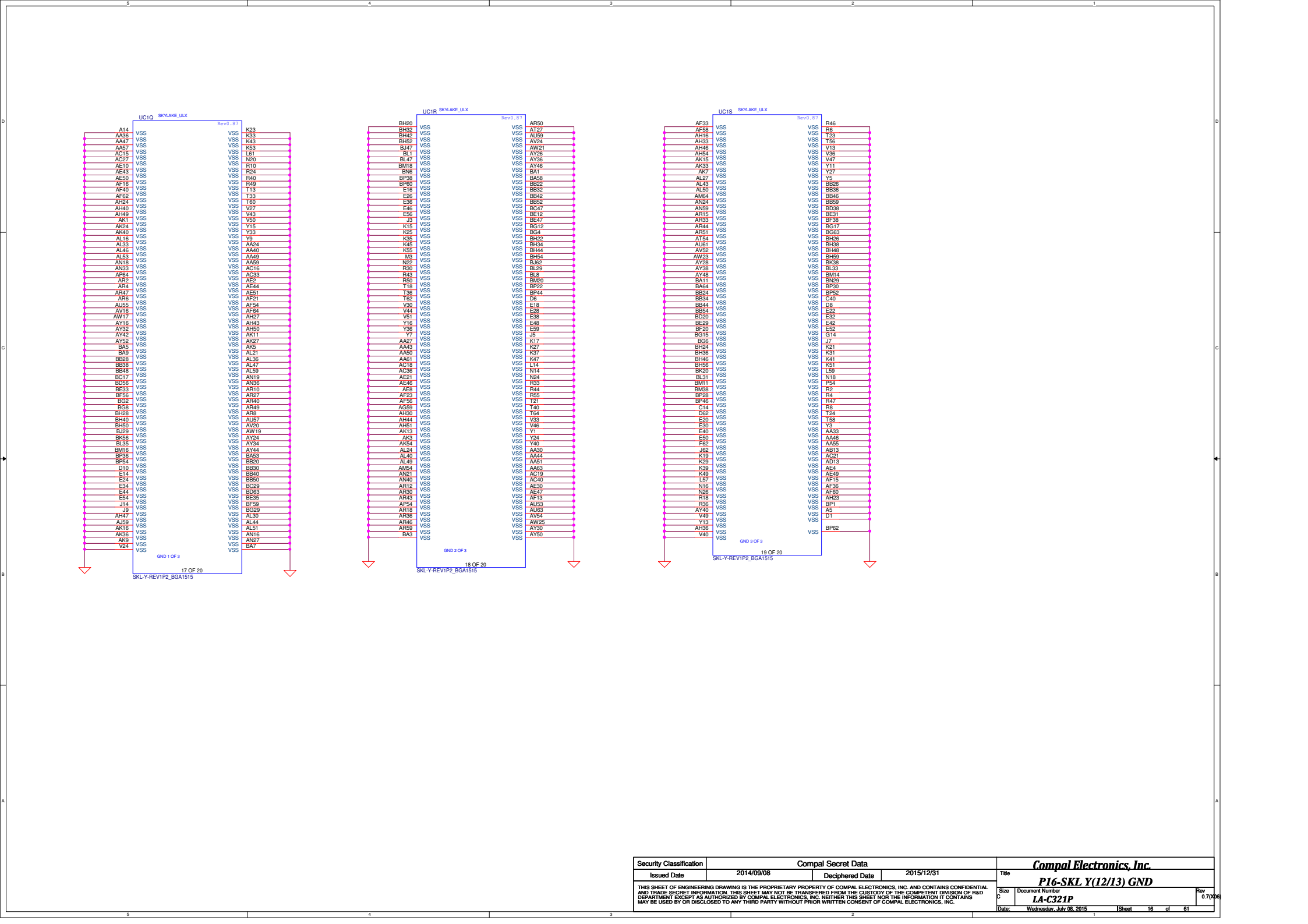


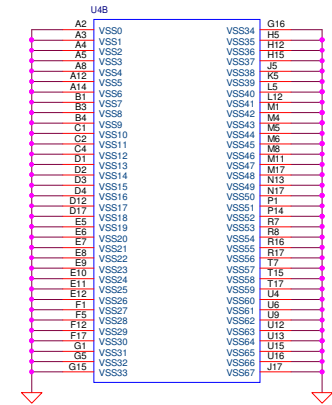
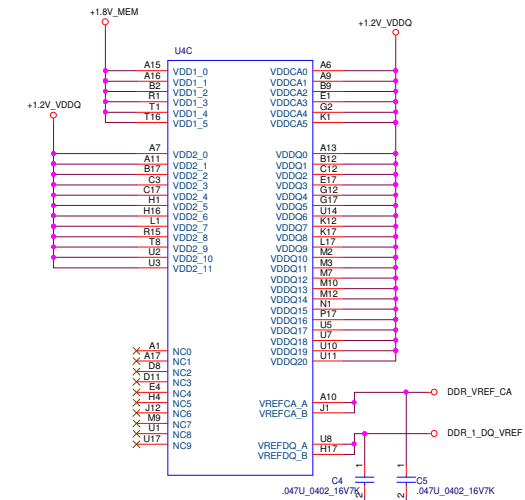
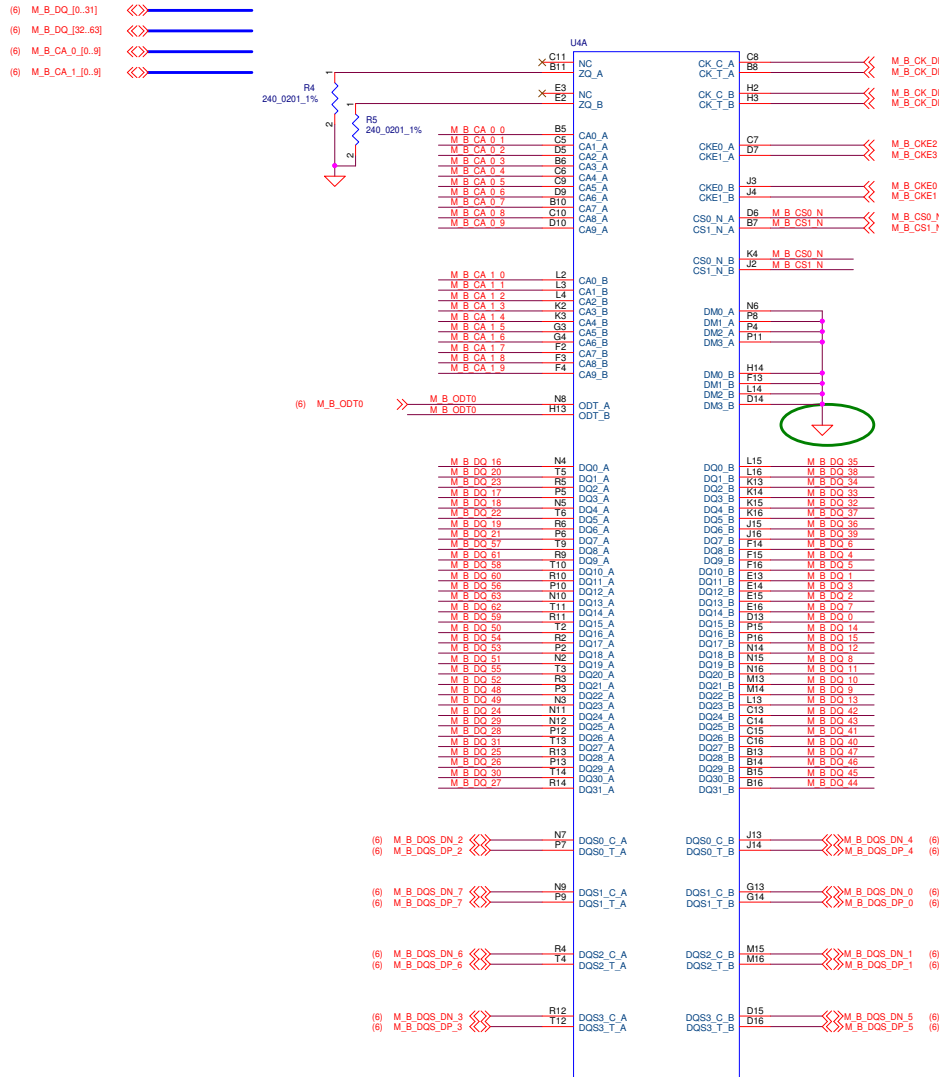
SVID CLK



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Date:	Wednesday, July 08, 2015	Sheet	14	of	61



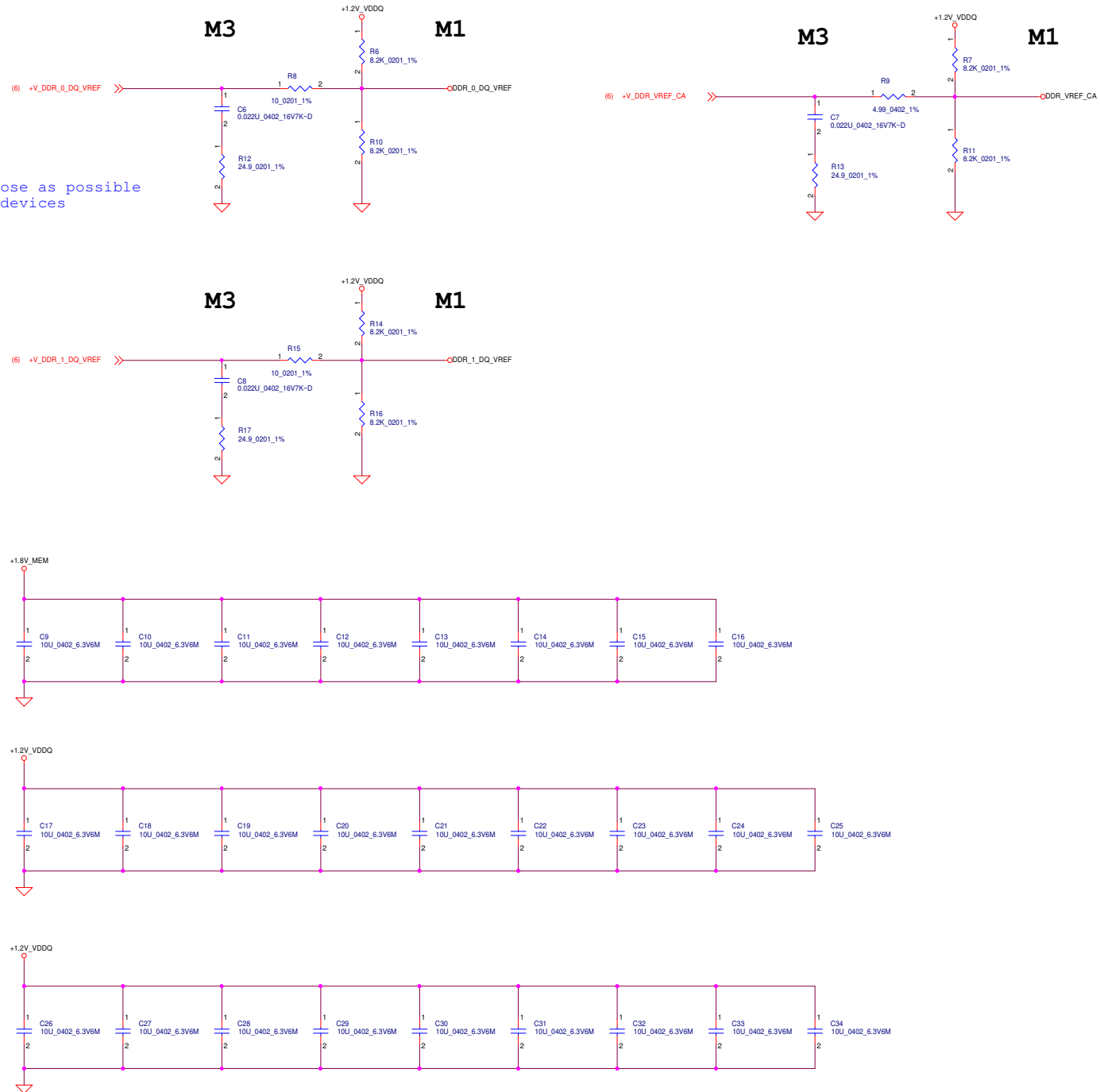






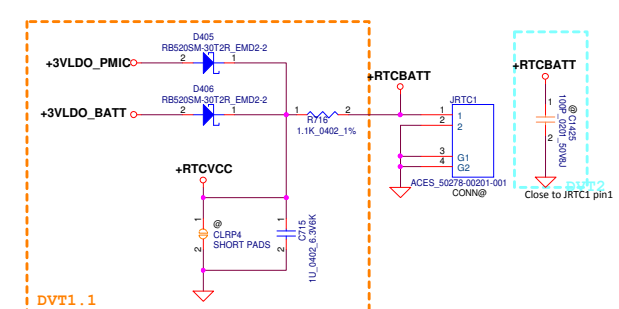
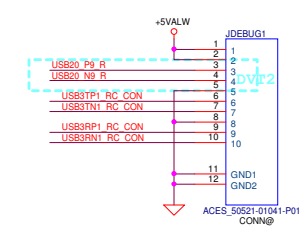
All VREF traces should have 10 mil trace width

Place the VREF voltage divider as close as possible to the LPDDR3 x64 memory down DREM devices

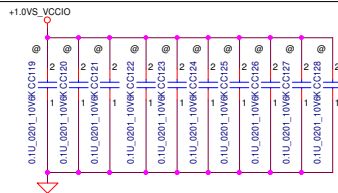
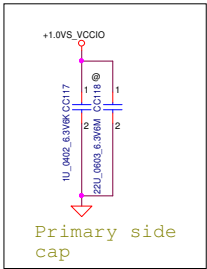
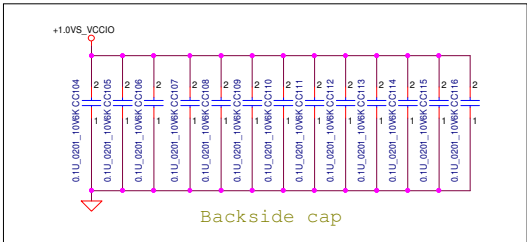
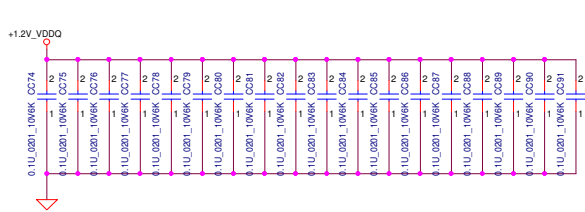
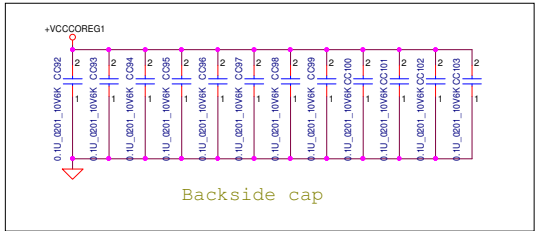
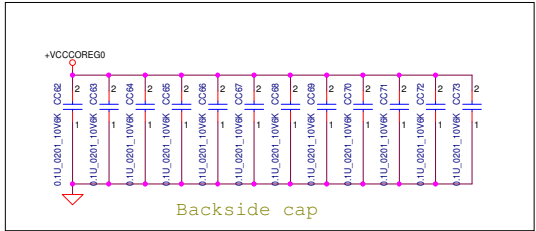


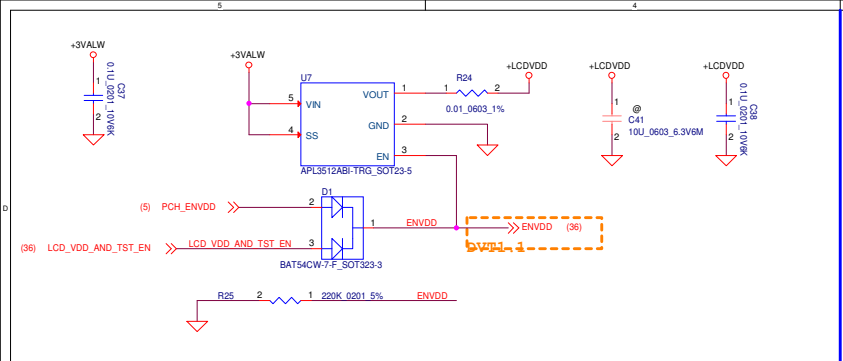
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				Date	Wednesday, July 09, 2015
				Sheet	20 of 61

RTC

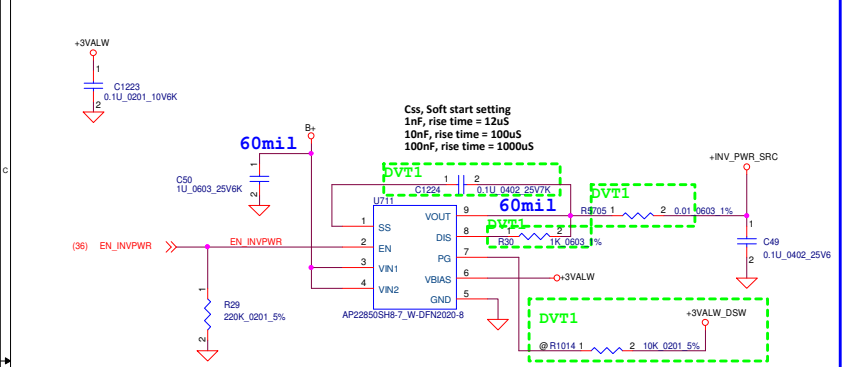


Security Classification		Compal Secret Data		<div>Compal Electronics, Inc.</div>	
Issued Date	2014/09/08	Deciphered Date	2013/10/28	<div>Title</div> <div>P21-XDP,APS,Debug CONN</div>	
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				Date	<div>Wednesday, July 08, 2015</div> <div>Sheet 21 of 61</div>

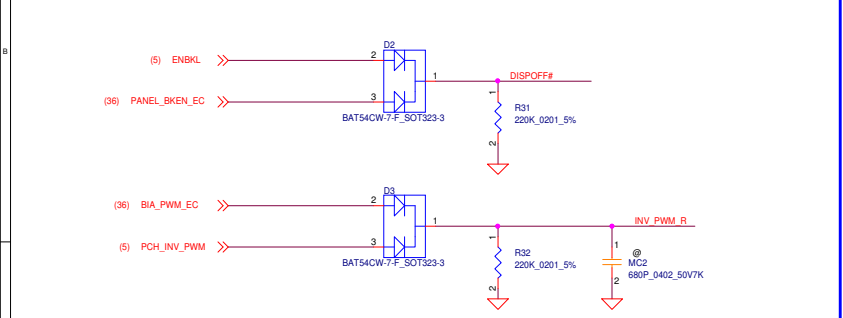




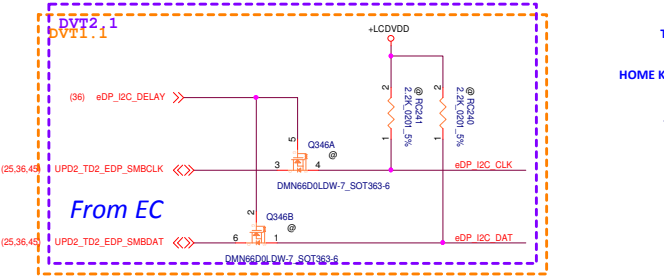
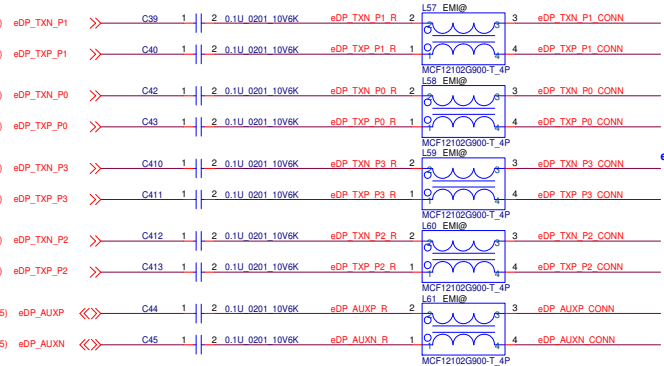
eDP BackLight Power



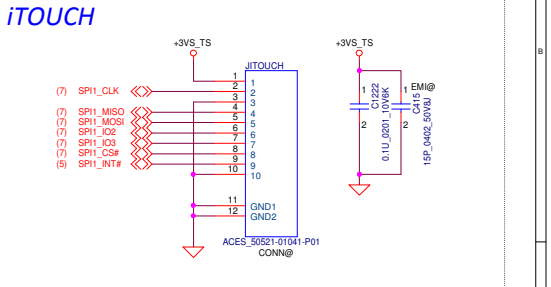
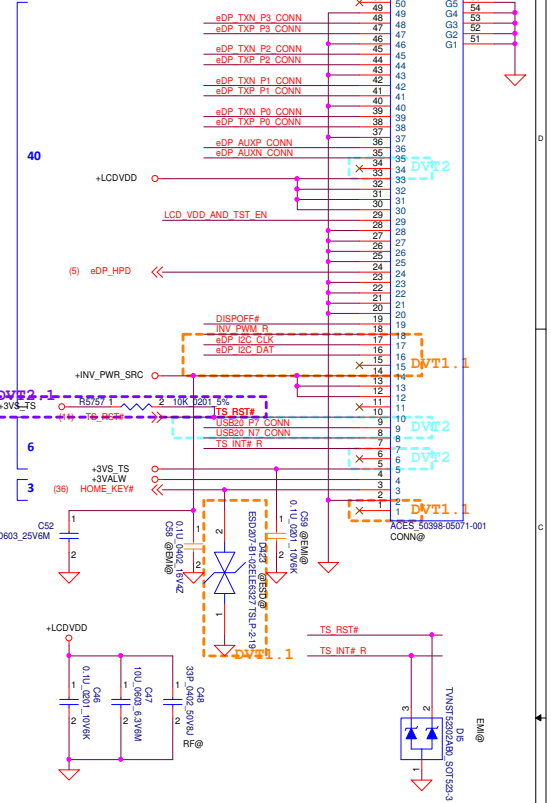
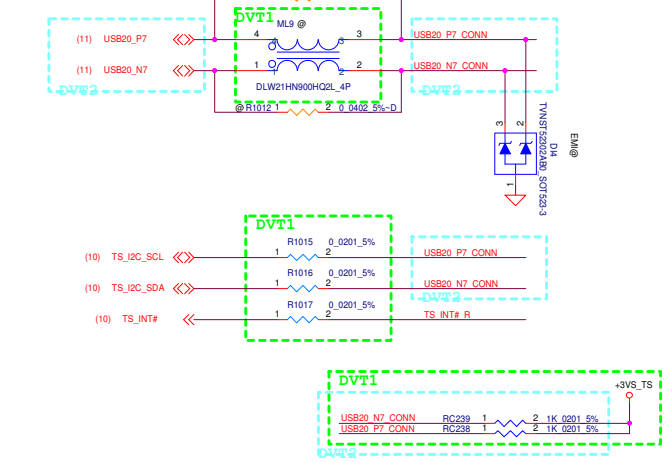
BackLight PWM Control



eDP Conn

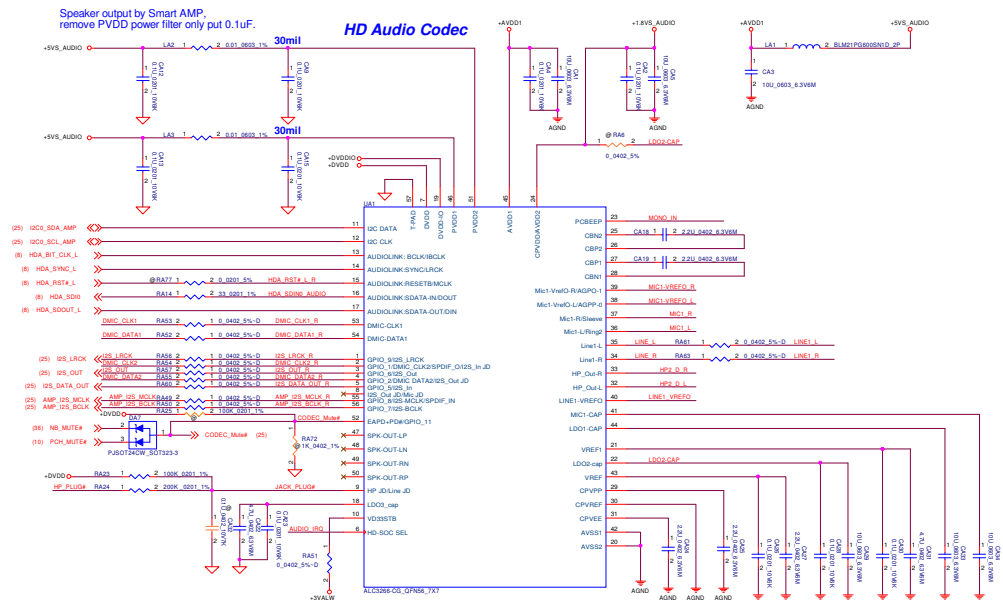


Touch Screen (Co-lay with I2C interface)

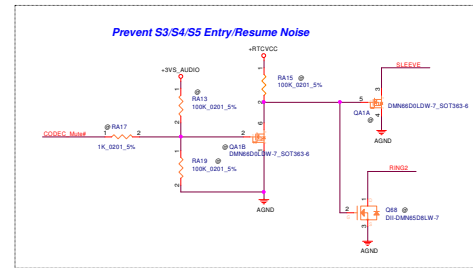


Speaker output by Smart AMP.
remove PVDD power filter only put 0.1uF.

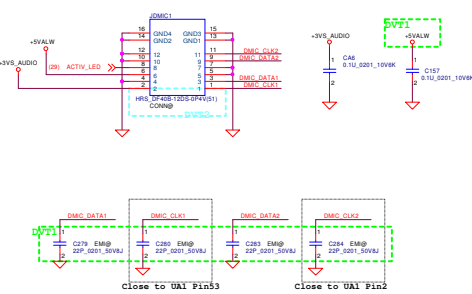
HD Audio Codec



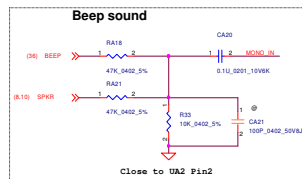
Prevent S3/S4/S5 Entry/Resume Noise



DMICS/CAMERA LED



Beep sound

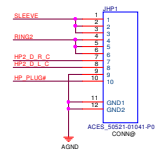
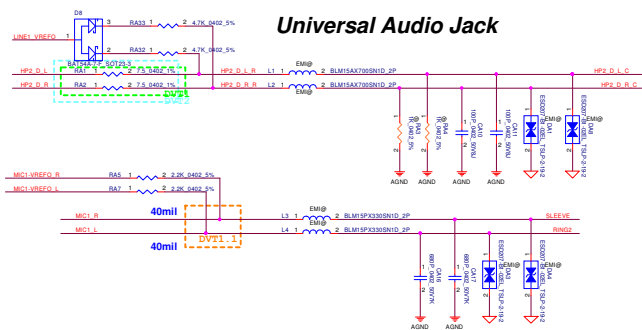


Codec

Analog
Pin20-45

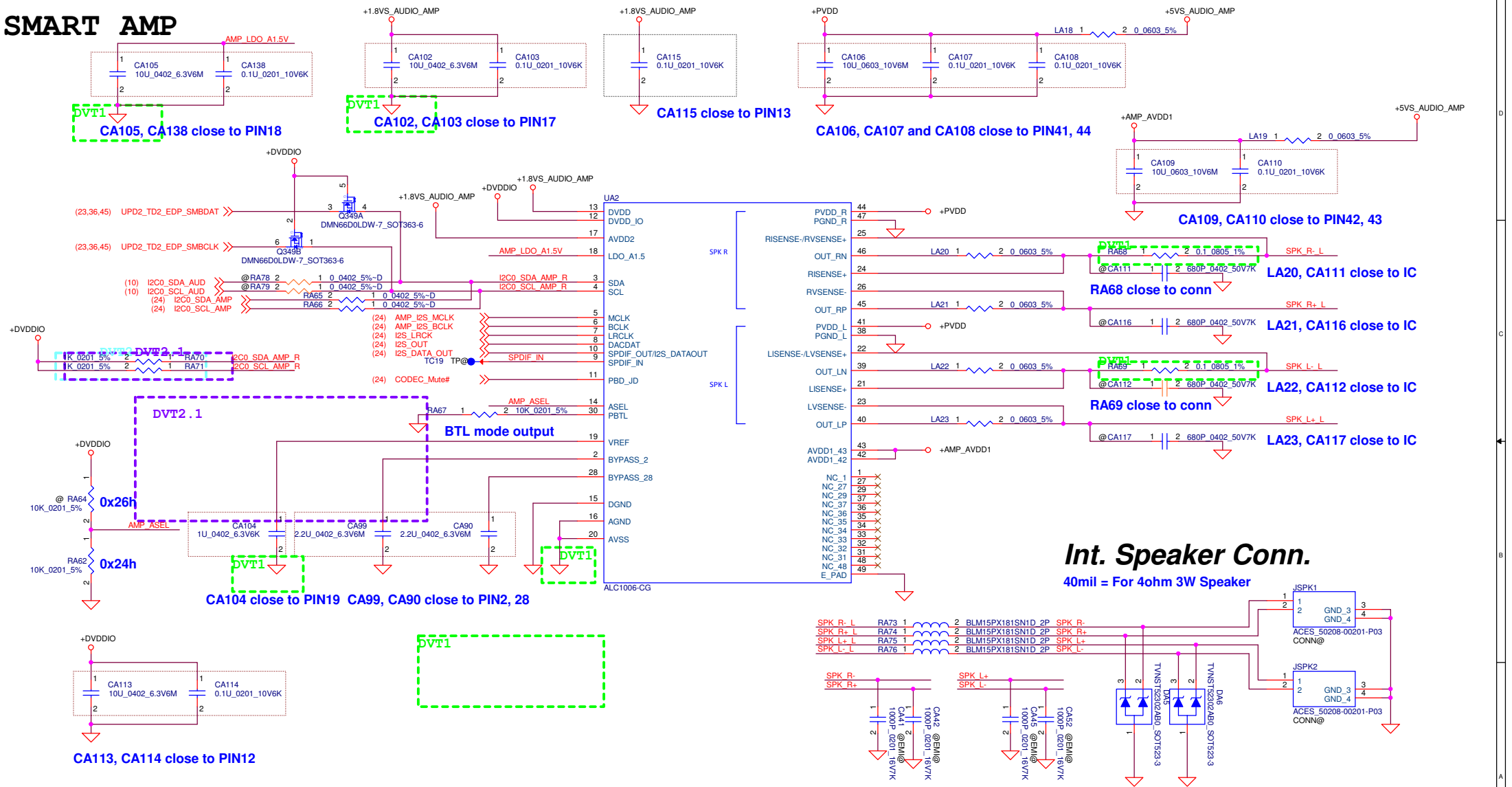
Digital
Pin1-19, 46-56

Universal Audio Jack



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Rev	P24-Audio Codec3266	Rev	0.1/000
Rev	LA-C321P	Rev	0.1/000
Rev	Washington, DC, US, 2015	Rev	24 of 81

SMART AMP

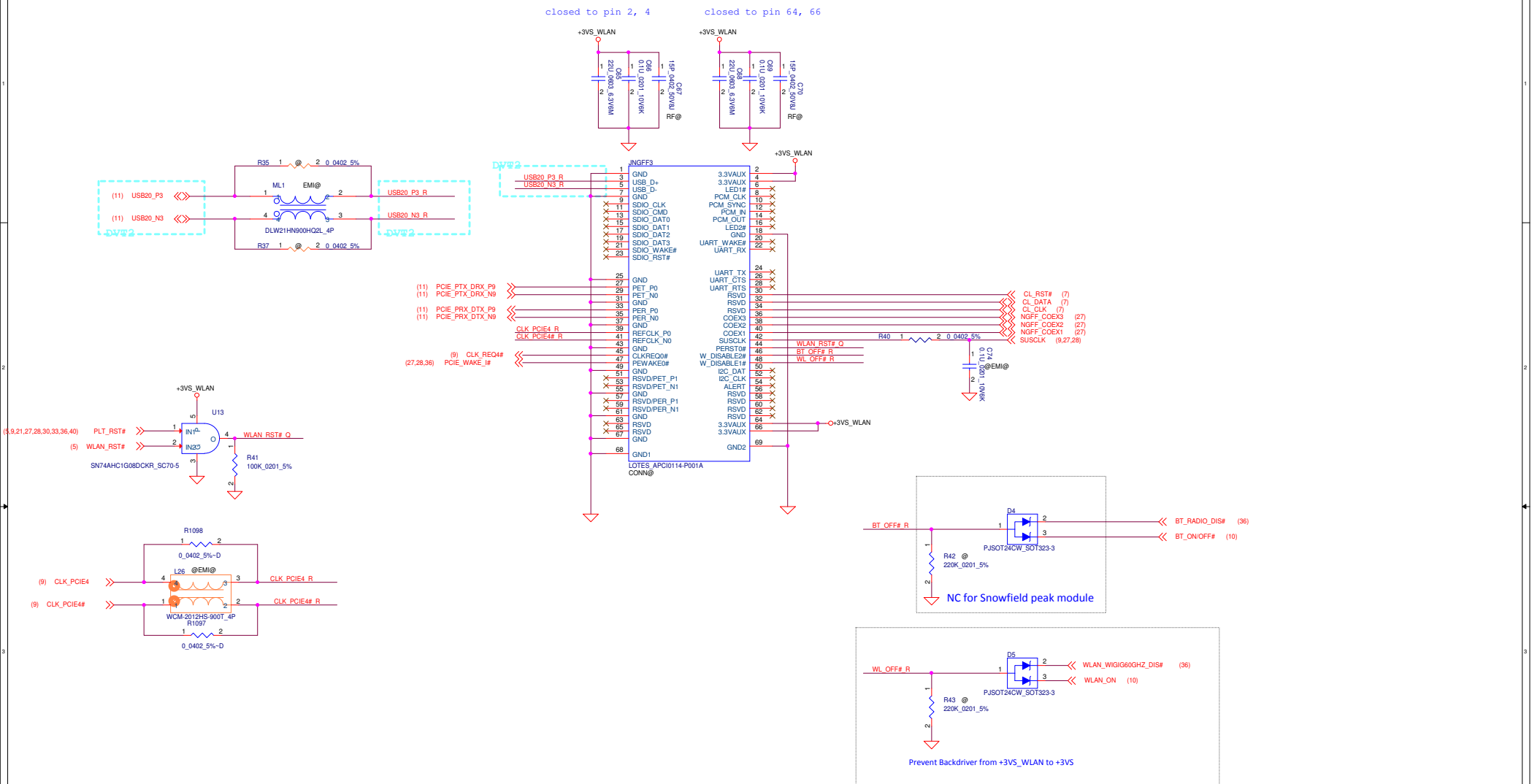


Int. Speaker Conn.

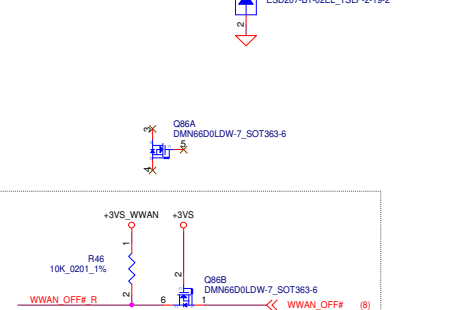
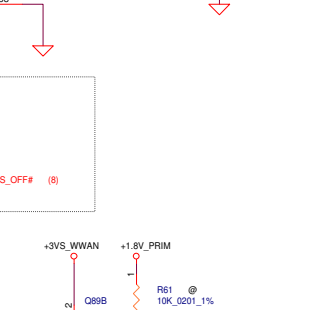
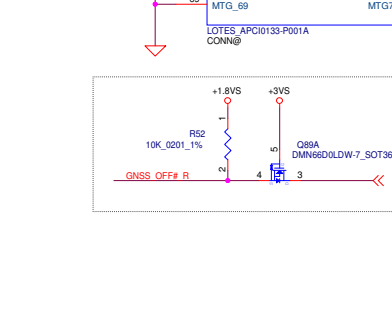
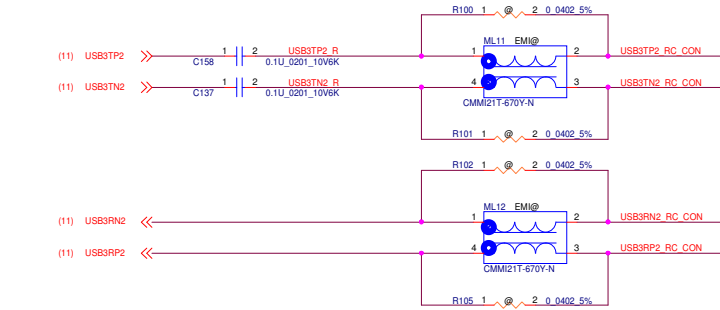
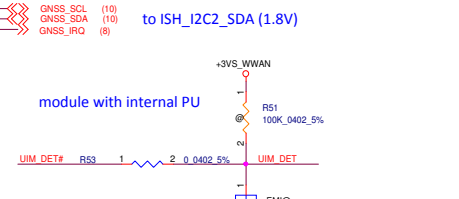
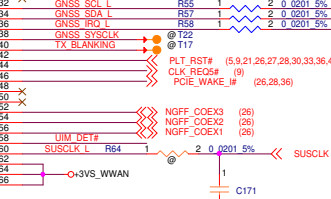
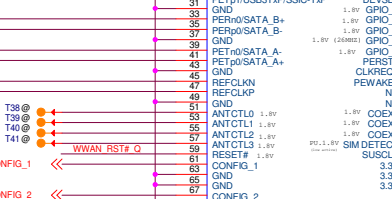
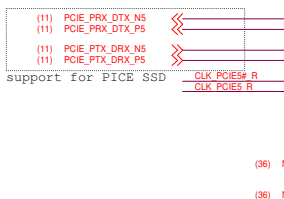
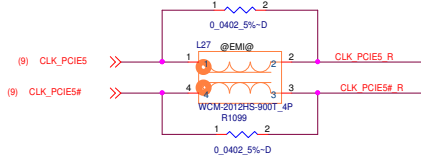
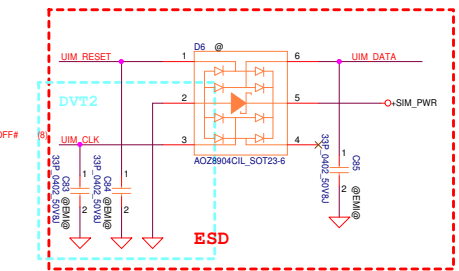
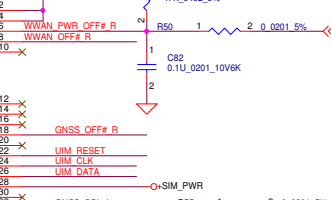
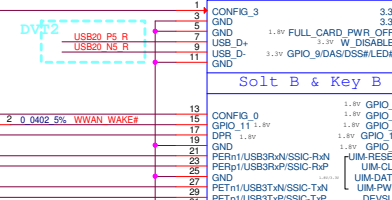
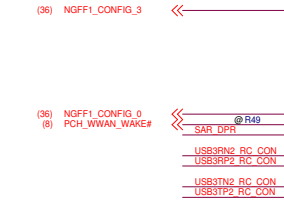
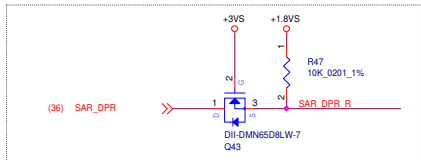
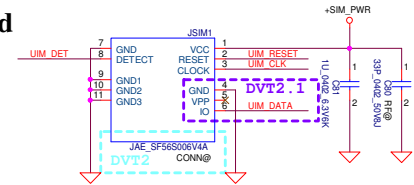
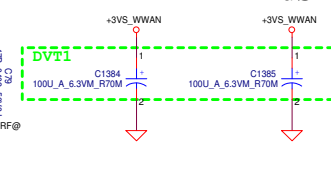
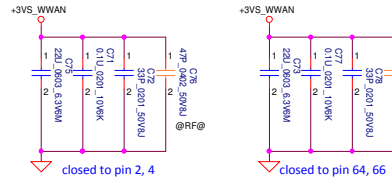
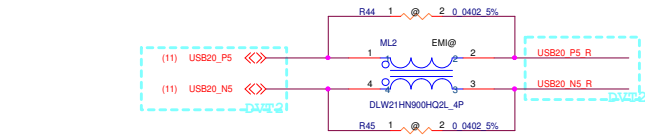
40ml = For 4ohm 3W Speaker

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				Date	Wednesday, July 08, 2015
				Sheet	25 of 61

Wireless LAN

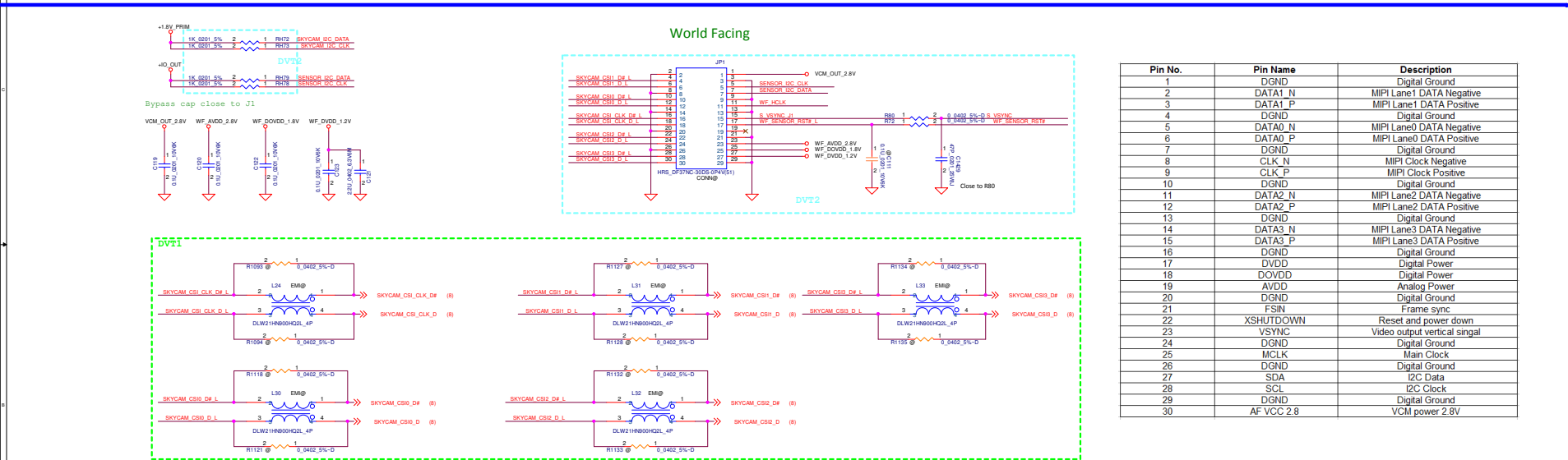


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				LA-C321P Date: Wednesday, July 08, 2015 Sheet 26 of 61	

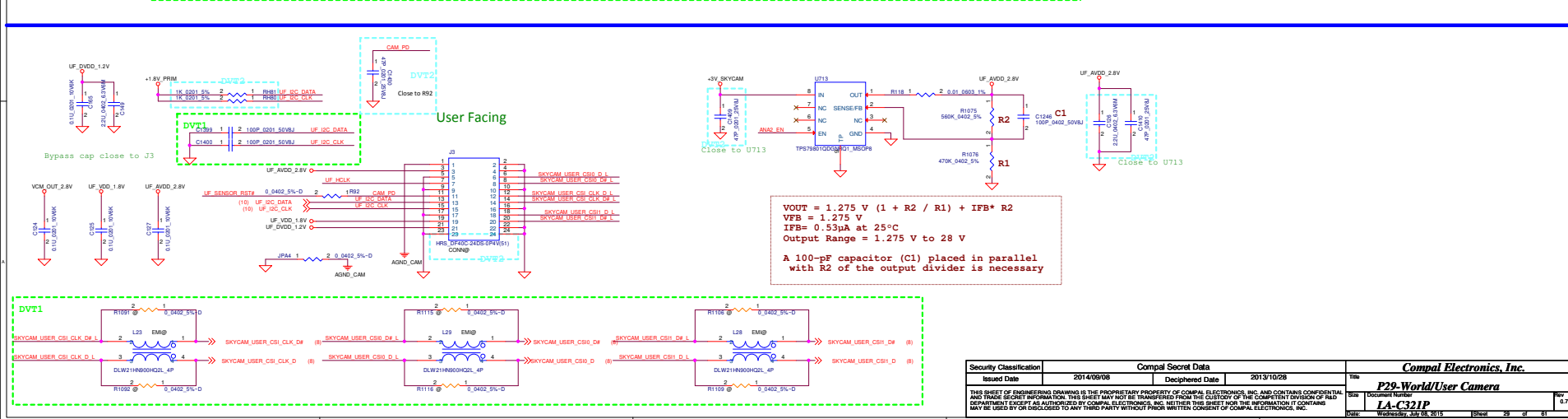


State#	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type	Port Configuration
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	HIGH	GND	GND	SSD - PCIe	N/A
2	GND	GND	HIGH	GND	WWAN - PCIe	0
3	GND	HIGH	HIGH	GND	WWAN - PCIe	1
4	GND	GND	GND	HIGH	WWAN - USB 3.0	0
5	GND	HIGH	GND	HIGH	WWAN - USB 3.0	1
6	GND	GND	HIGH	HIGH	WWAN - USB 3.0	2
7	GND	HIGH	HIGH	HIGH	WWAN - USB 3.0	3
8	HIGH	GND	GND	GND	WWAN - SSIC	0
9	HIGH	HIGH	GND	GND	WWAN - SSIC	1
10	HIGH	GND	HIGH	GND	WWAN - SSIC	2
11	HIGH	HIGH	HIGH	GND	WWAN - SSIC	3
12	HIGH	GND	GND	HIGH	WWAN - PCIe	2
13	HIGH	HIGH	GND	HIGH	WWAN - PCIe	3
14	HIGH	GND	HIGH	HIGH	DDP HCA - PCIe	N/A
15	HIGH	HIGH	HIGH	HIGH	No Module	N/A

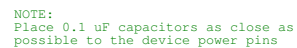
Pin	Port Config_0	Port Config_1	Port Config_2	Port Config_3
GPIO_0	40	GNSS_SCL	SIM_DET2	IPC_0
GPIO_1	42	GNSS_SDA	UIM_DTA2	IPC_1
GPIO_2	44	GNSS_IRQ	UIM_CLK2	IPC_2
GPIO_3	46	SYSLCK	UIM_RST2	IPC_3
GPIO_4	48	TX_BLANKING	UIM_PWR2	IPC_4
GPIO_5	20	AUDIO_0	RFU	AUDIO_0
GPIO_6	22	AUDIO_1	RFU	AUDIO_1
GPIO_7	24	AUDIO_2	RFU	IPC_5/AUDIO_2
GPIO_8	28	AUDIO_3	RFU	IPC_6/AUDIO_3
GPIO_9	10	LED_1#	LED_1#	IPC_7
GPIO_10	26	W_DISABLE2#	W_DISABLE2#	HSIC_STROBE
GPIO_11	23	WAKE_ON_WWAN#	WAKE_ON_WWAN#	HSIC_DATA



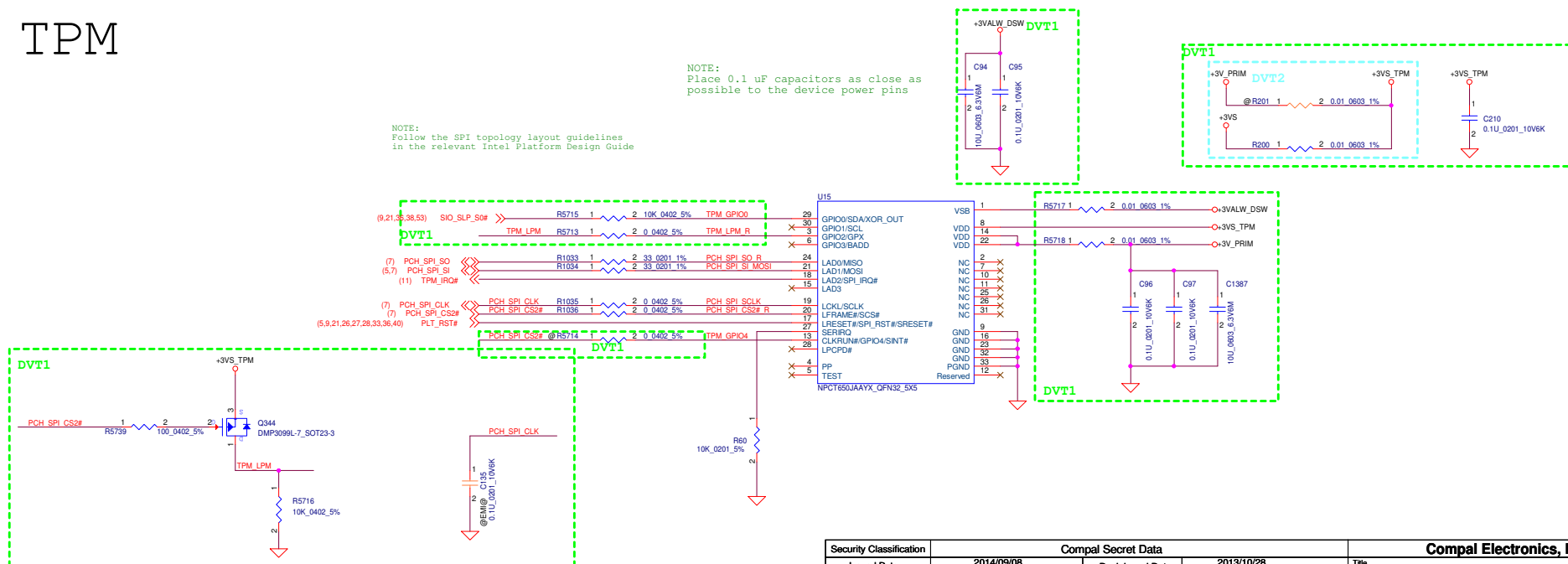
Pin No.	Pin Name	Description
1	DGND	Digital Ground
2	DAT1A1_N	MIPI Lane1 DATA Negative
3	DAT1A1_P	MIPI Lane1 DATA Positive
4	DGND	Digital Ground
5	DAT0A0_N	MIPI Lane0 DATA Negative
6	DAT0A0_P	MIPI Lane0 DATA Positive
7	DGND	Digital Ground
8	CLK_N	MIPI Clock Negative
9	CLK_P	MIPI Clock Positive
10	DGND	Digital Ground
11	DAT2A2_N	MIPI Lane2 DATA Negative
12	DAT2A2_P	MIPI Lane2 DATA Positive
13	DGND	Digital Ground
14	DAT3A3_N	MIPI Lane3 DATA Negative
15	DAT3A3_P	MIPI Lane3 DATA Positive
16	DGND	Digital Ground
17	DVDD	Digital Power
18	D0VDD	Digital Power
19	AVDD	Analog Power
20	DGND	Digital Ground
21	FSIN	Frame sync
22	XSHUTDOWN	Reset and power down
23	VSYNCR	Video output vertical singal
24	DGND	Digital Ground
25	MCLK	Main Clock
26	DGND	Digital Ground
27	SDA	I2C Data
28	SCL	I2C Clock
29	DGND	Digital Ground
30	AF VCC 2.8	VCM power 2.8V



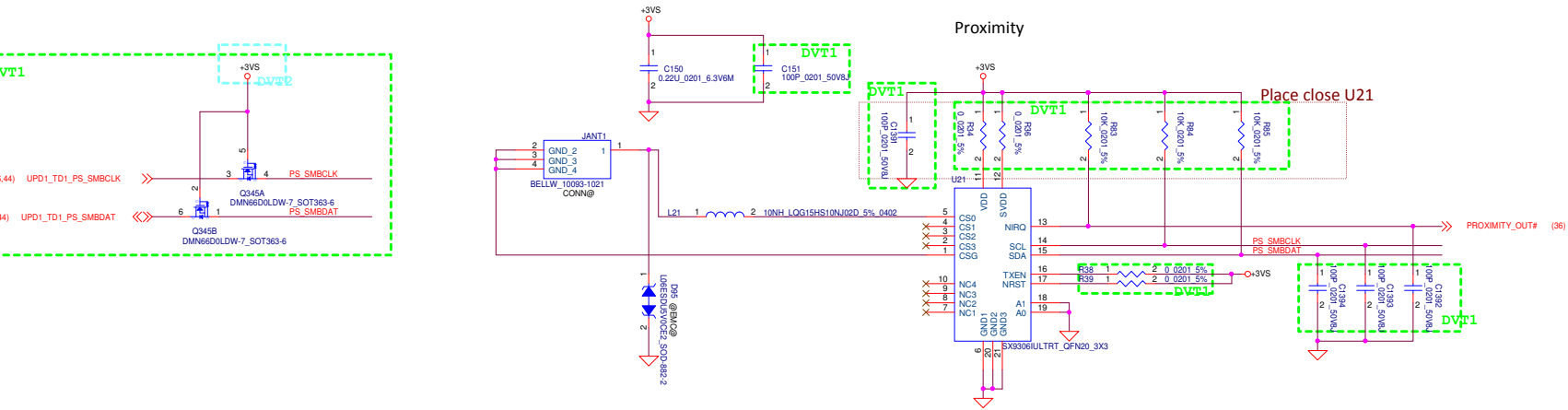
TPM



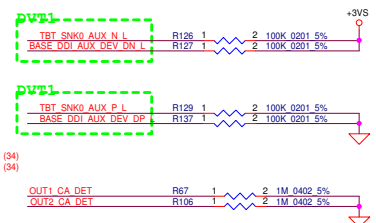
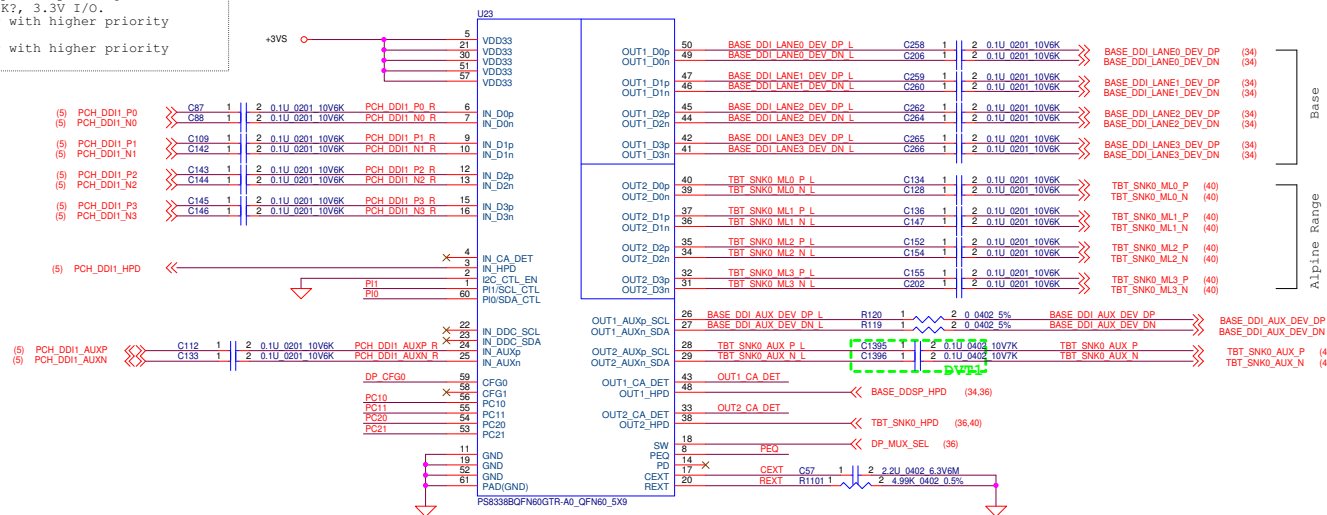
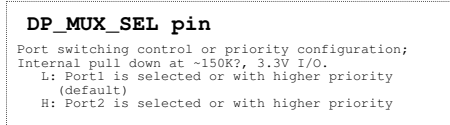
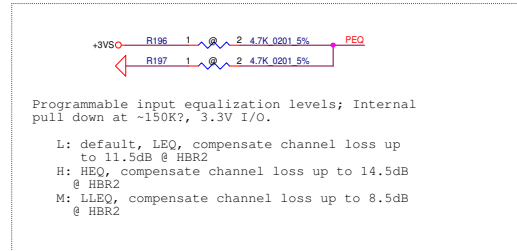
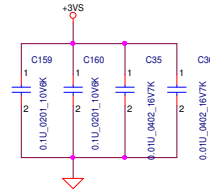
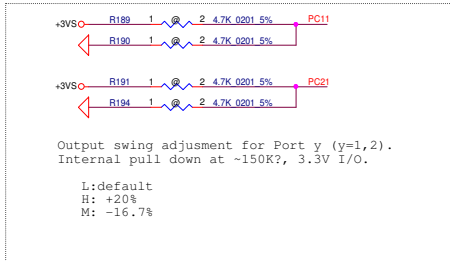
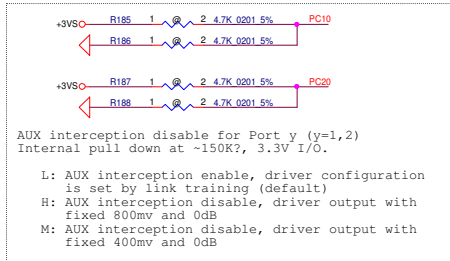
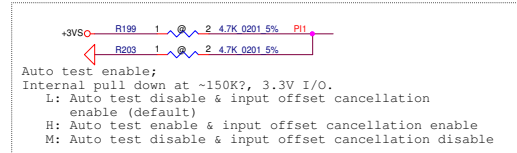
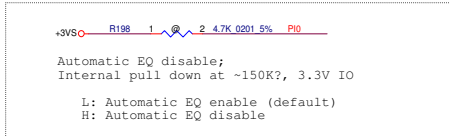
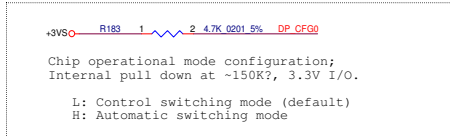
NOTE:
Follow the SPI topology layout guidelines
in the relevant Intel Platform Design Guide



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				C	LA-C321P	0.7/006
				Date:	Wednesday, July 08, 2015	Sheet 30 of 61

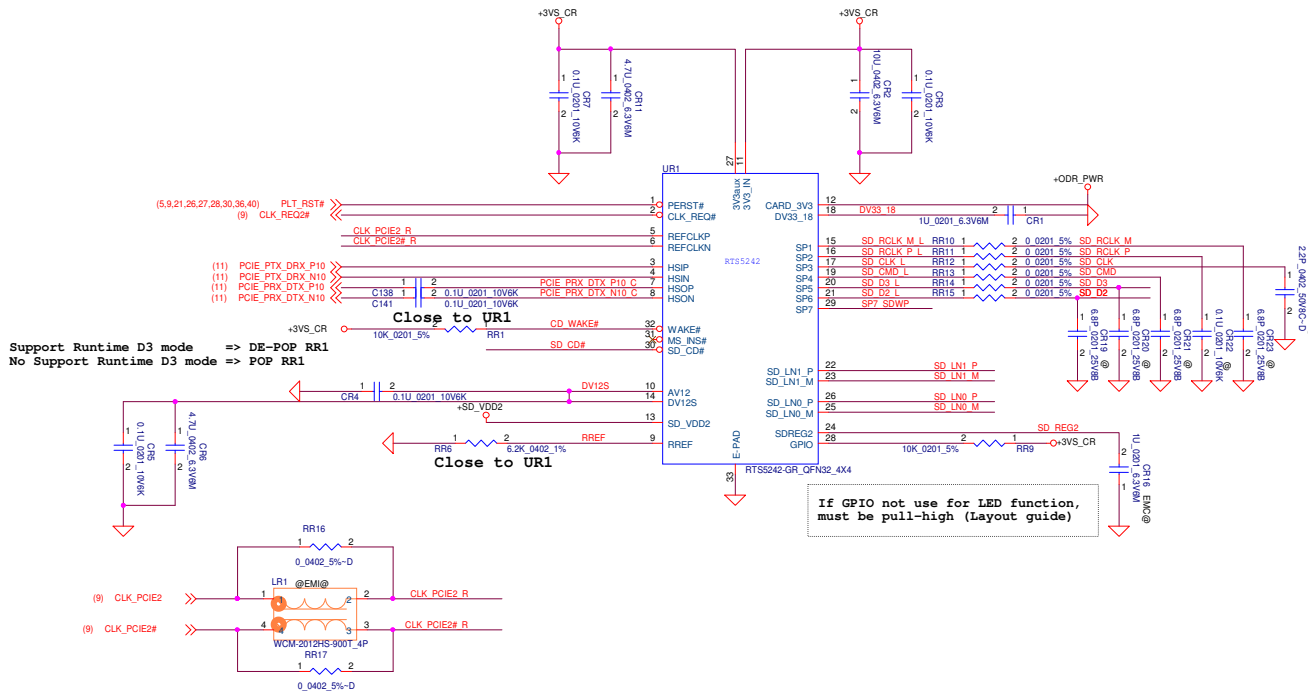
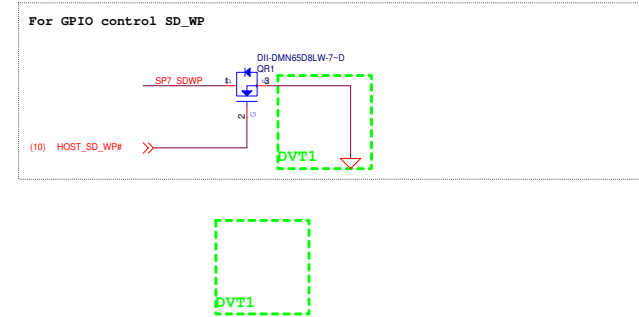
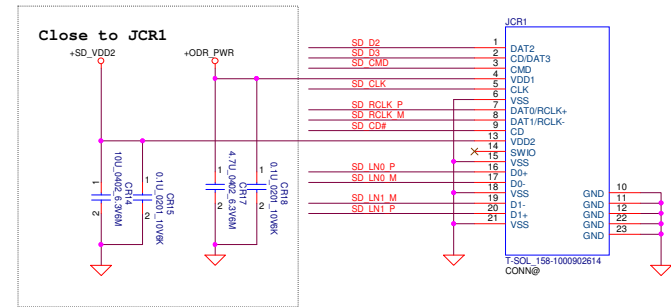


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				Size	Document Number LA-C321P
Date: Wednesday, July 08, 2015				Sheet	31 of 61



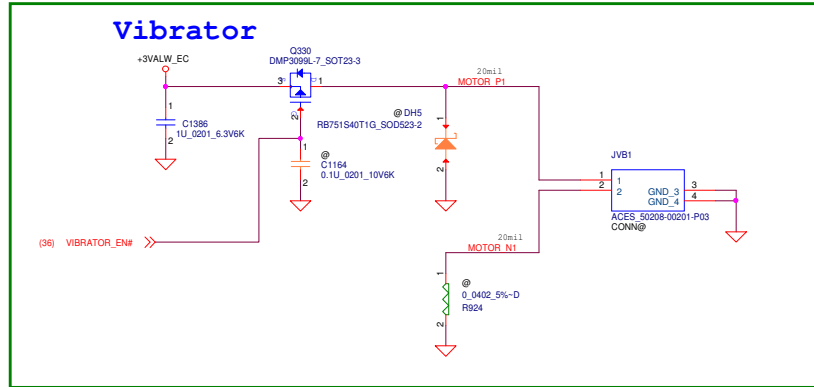
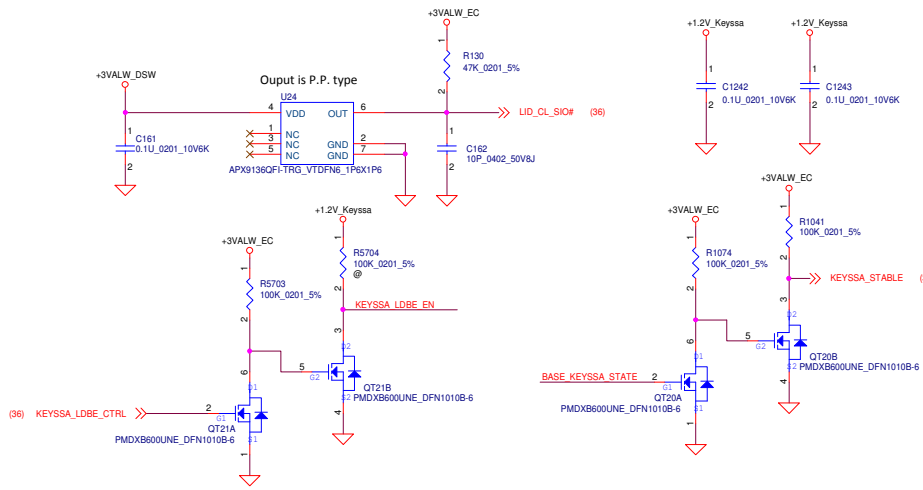
Card Reader

- 2) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
 - Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
 - Bulk capacitor for Card 3V3 place closed to flash card socket.
 - Bulk capacitor for 3V3_IN / 3V3aux / DV12S place closed to RTS5242 chip.
- 3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.

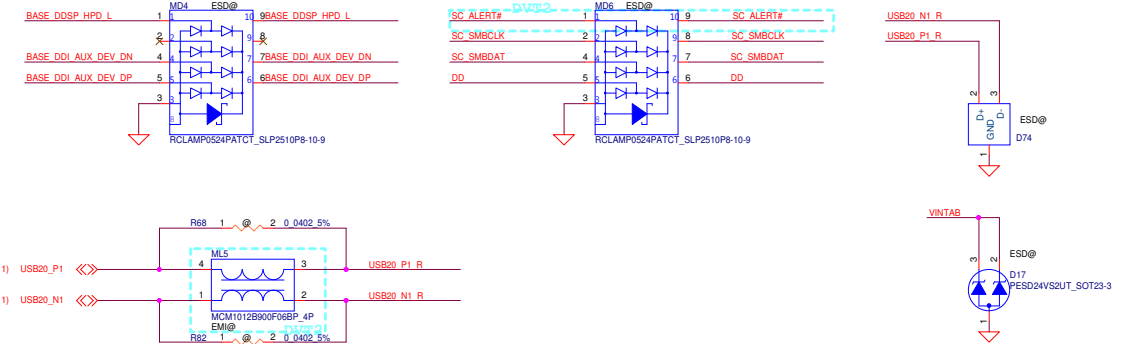
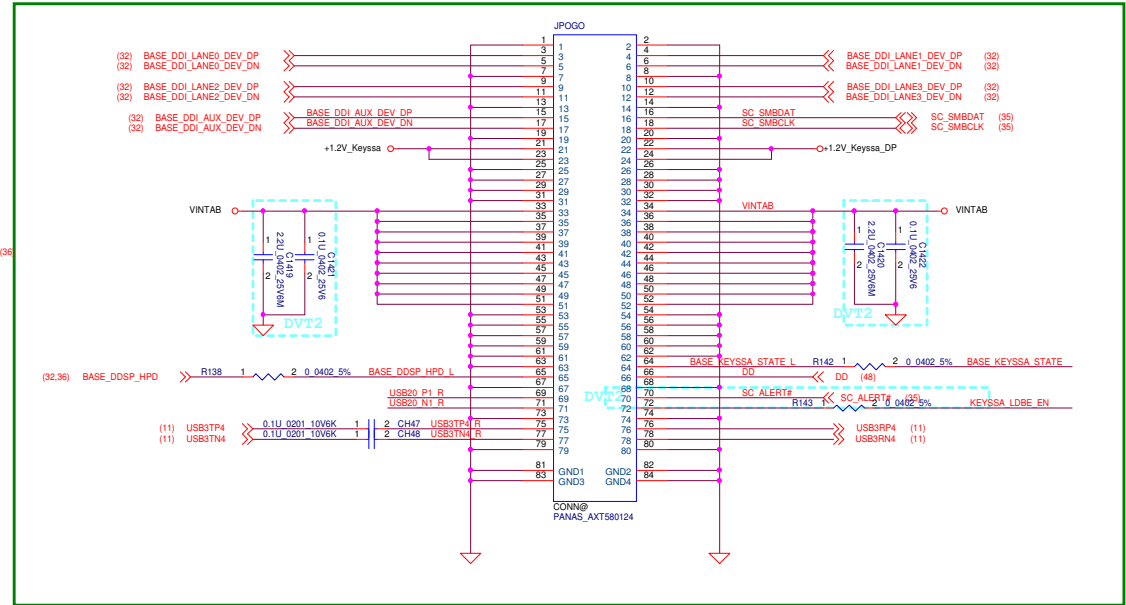


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Issued Date	2014/09/08	Deciphered Date	2012/07/25	Title	
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				Date:	Wednesday, July 08, 2015
				Sheet	33 of 61

LID SW

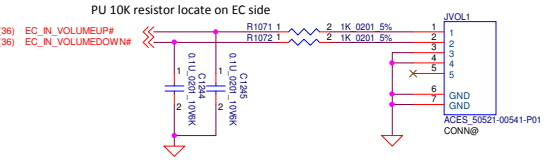
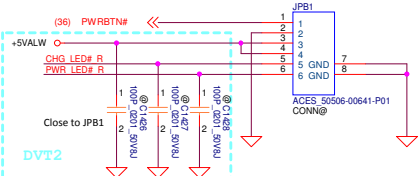
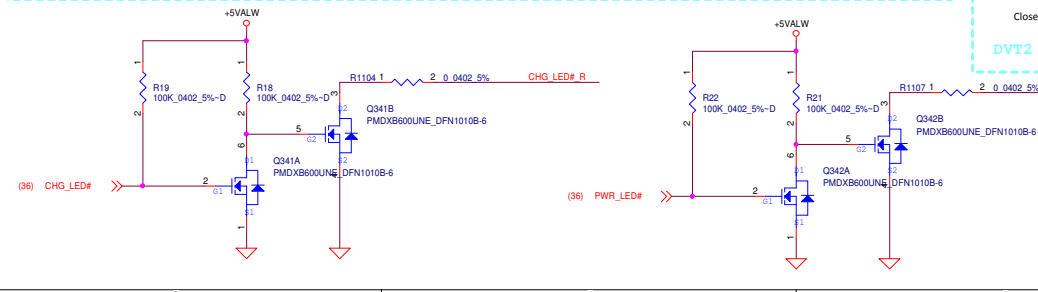
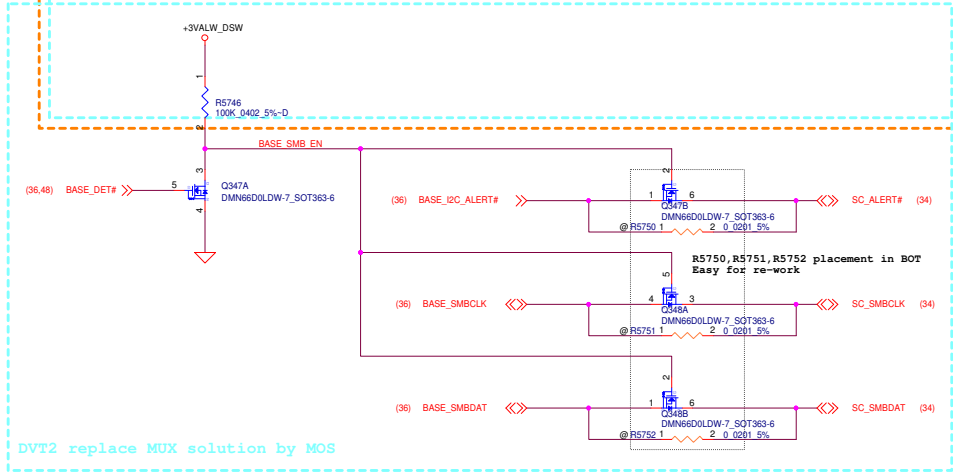


Keyssa USB3.0 and Displayport Conns

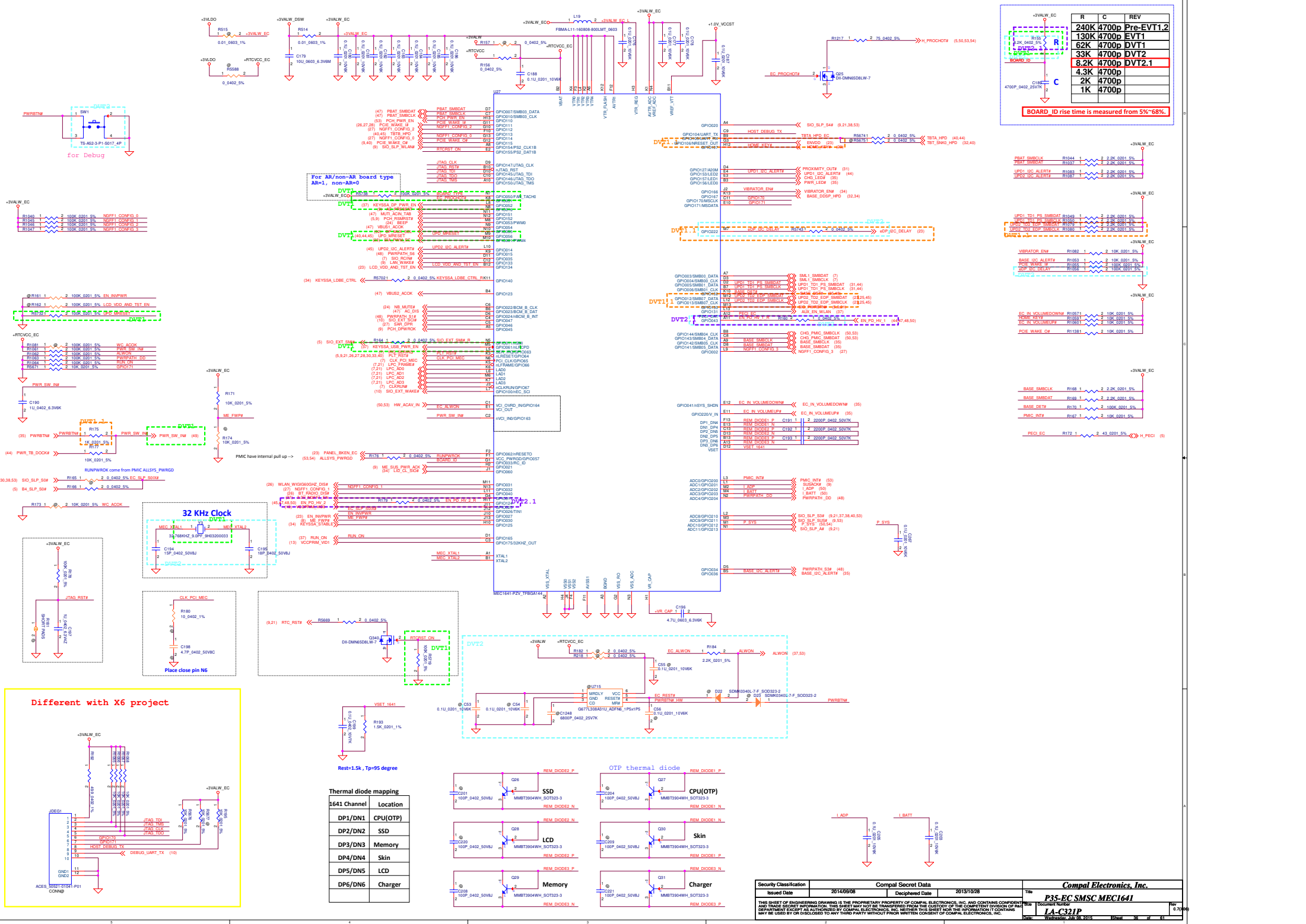


HEAD SIDE

DVT1.1 De-pop SB
DVT2 Remove SB



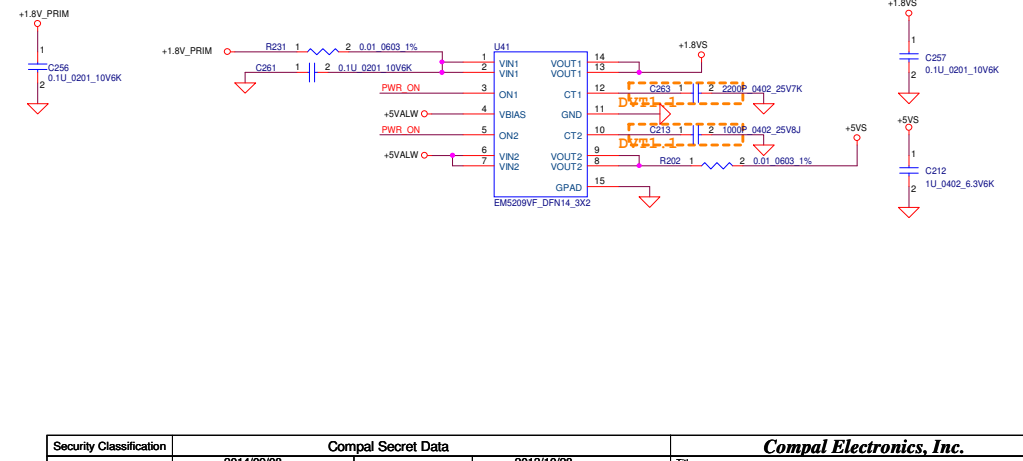
Security Classification	Compal Secret Data		Title	
Issued Date	2014/09/08	Deciphered Date	2013/10/28	P34-LatticeSB/PB/VOL Ctrl Conn
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				Rev 0.7(206)
				Date: Wednesday, July 08, 2015 1 Sheet 35 of 61



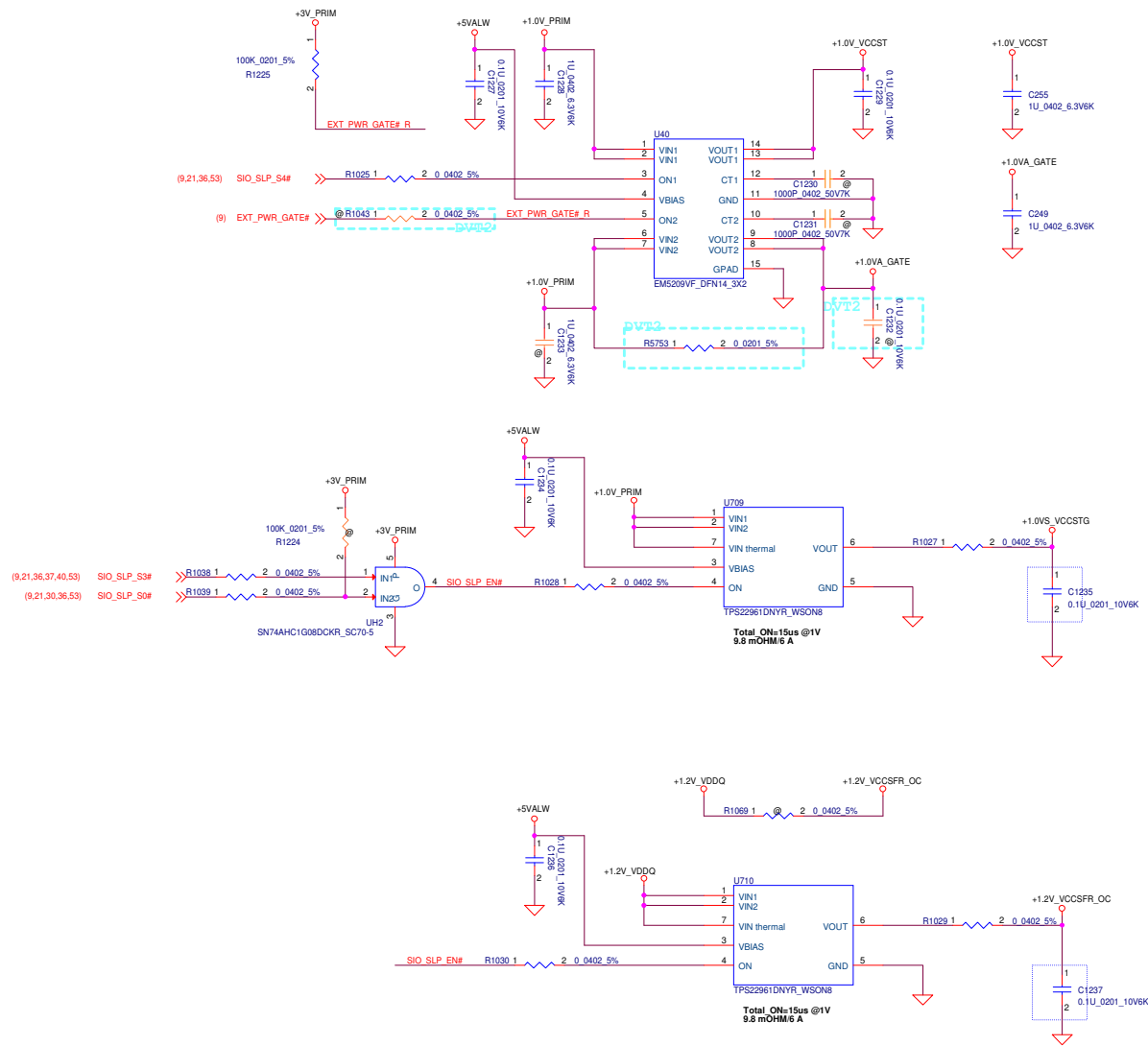
R	C	REV
240K	4700p	Pre-EVT1.2
130K	4700p	EVT1
62K	4700p	DVT1
33K	4700p	DVT2
8.2K	4700p	DVT2.1
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD ID rise time is measured from 5%~68%.

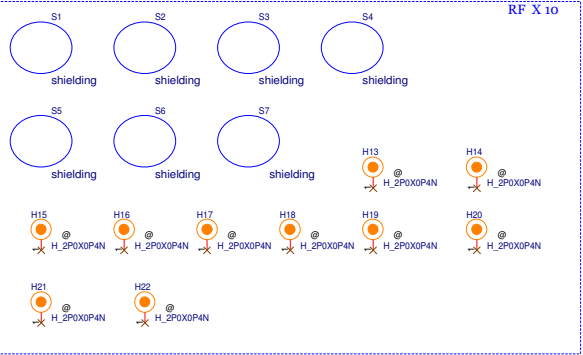
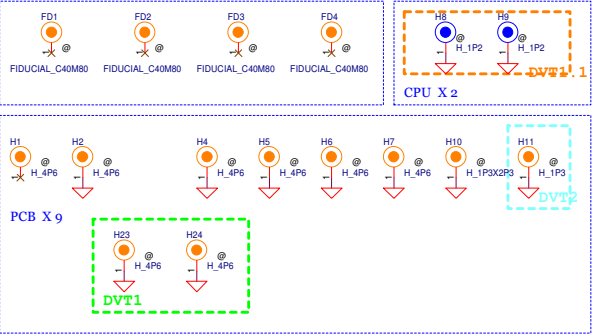
1641 Channel	Location
DP1/DN1	CPU(OTP)
DP2/DN2	SSD
DP3/DN3	Memory
DP4/DN4	Skin
DP5/DN5	LCD
DP6/DN6	Charger



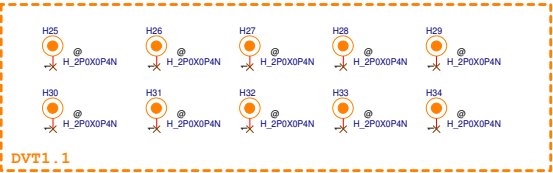
Security Classification	Compal Secret Data			Compal Electronics, Inc. P36-DC/DC Interface 1		
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					LA-C321P	0.7(008)
				Date:	Wednesday, Jul 08, 2015	Sheet 37 of 61



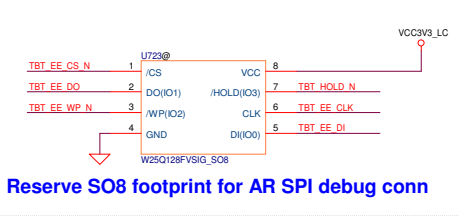
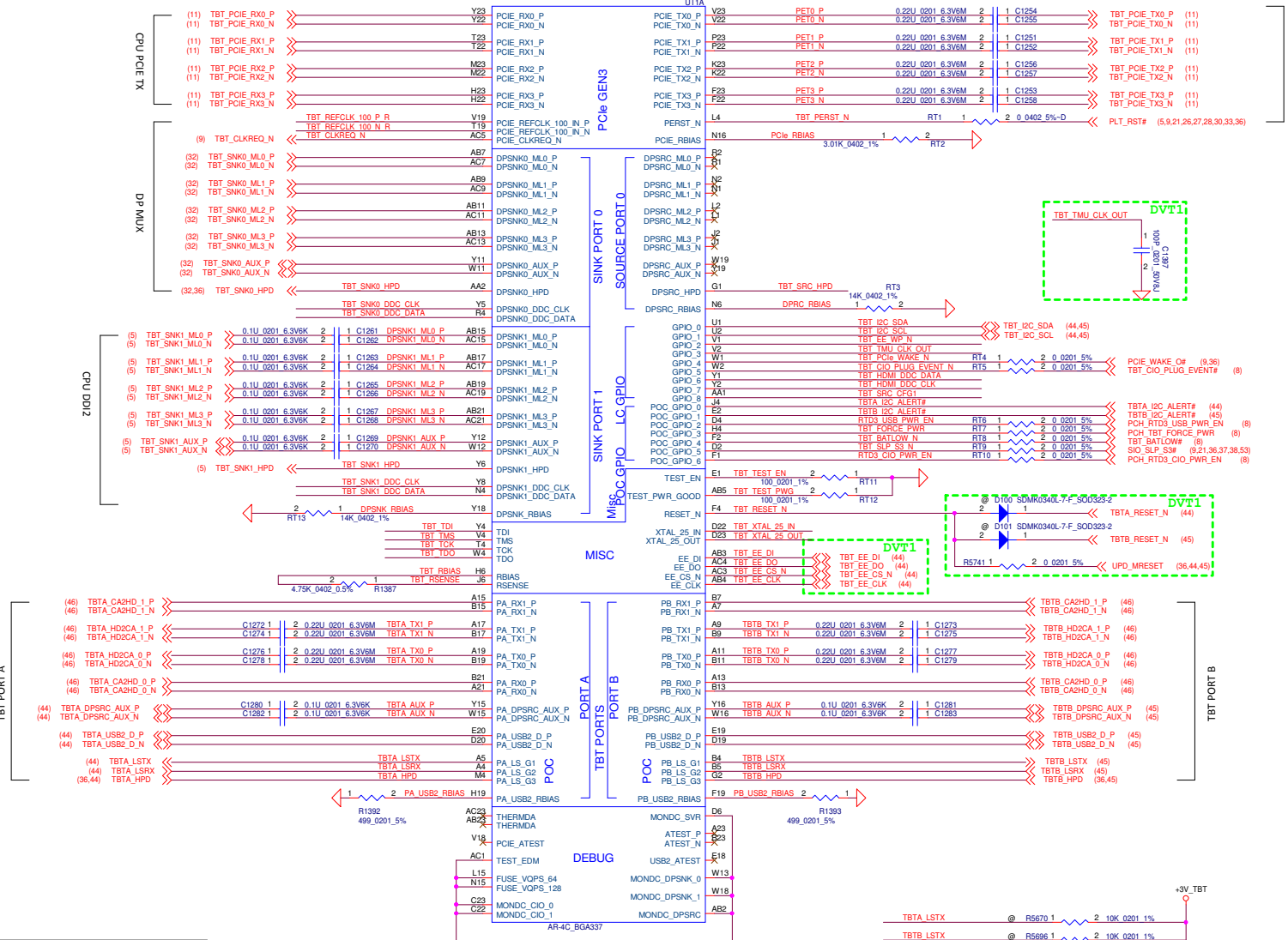
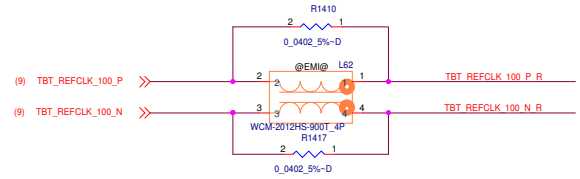
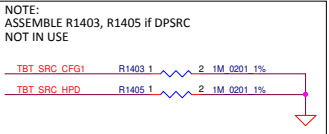
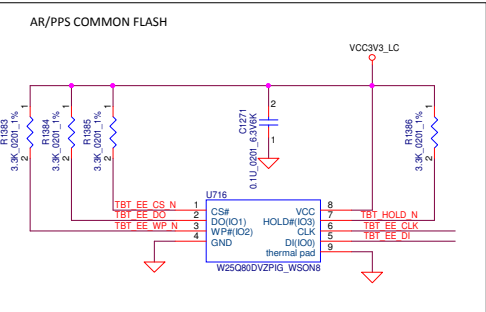
Screw Hole

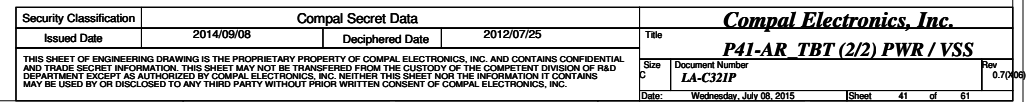


DVT1

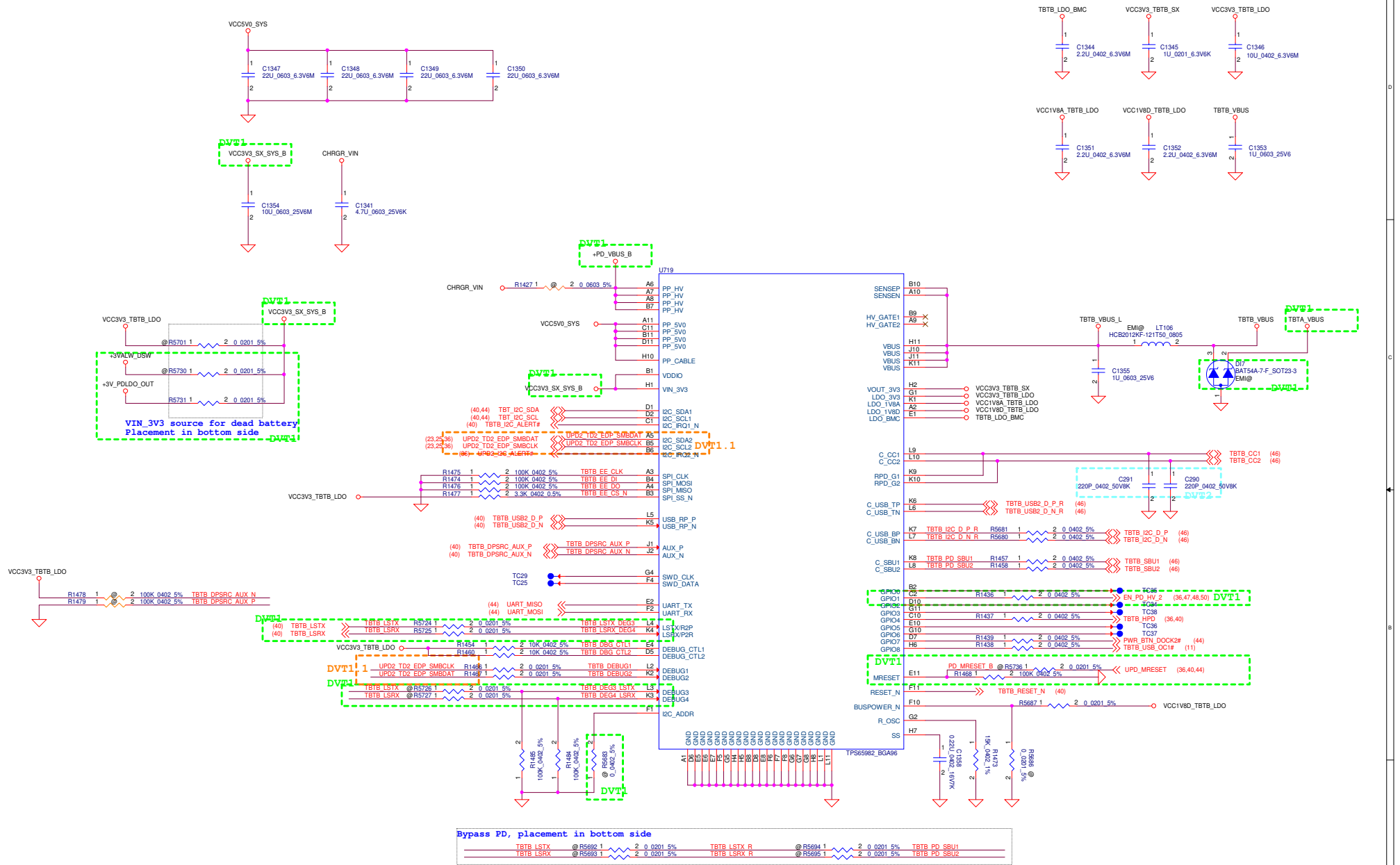


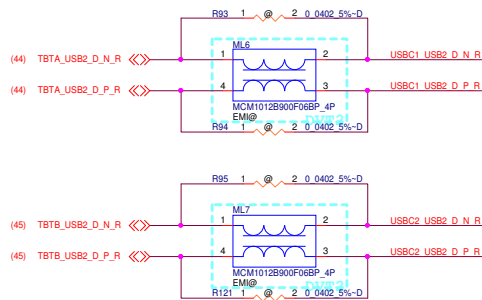
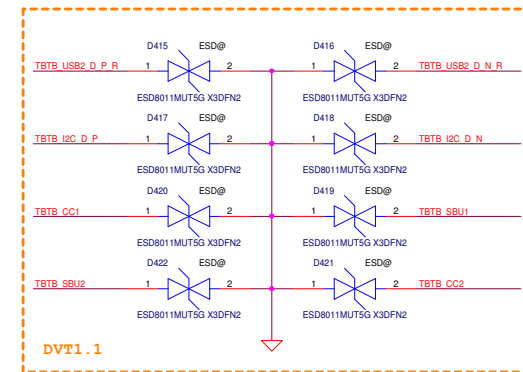
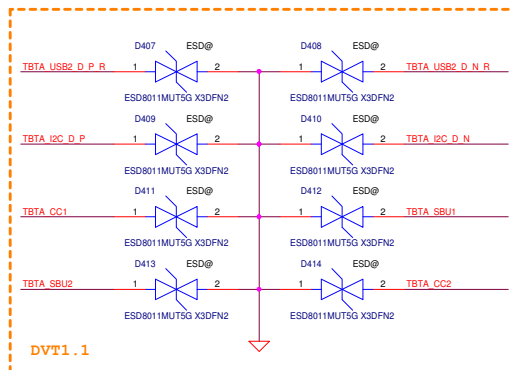
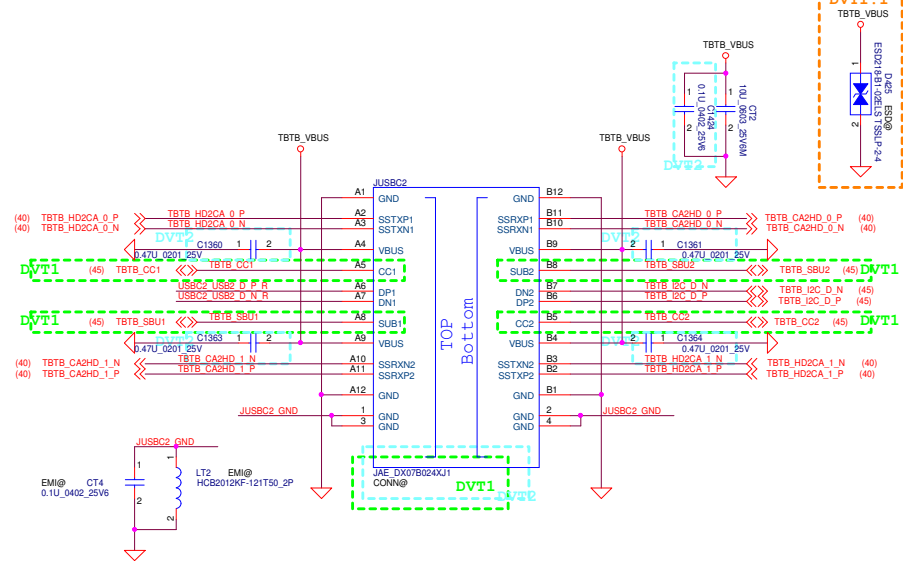
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Issued Date	2014/09/08	Deciphered Date	2013/10/28	Title	
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					LA-C321P
				Date:	Wednesday, July 09, 2015
				Sheet	39 of 61
				Rev	0.7(206)



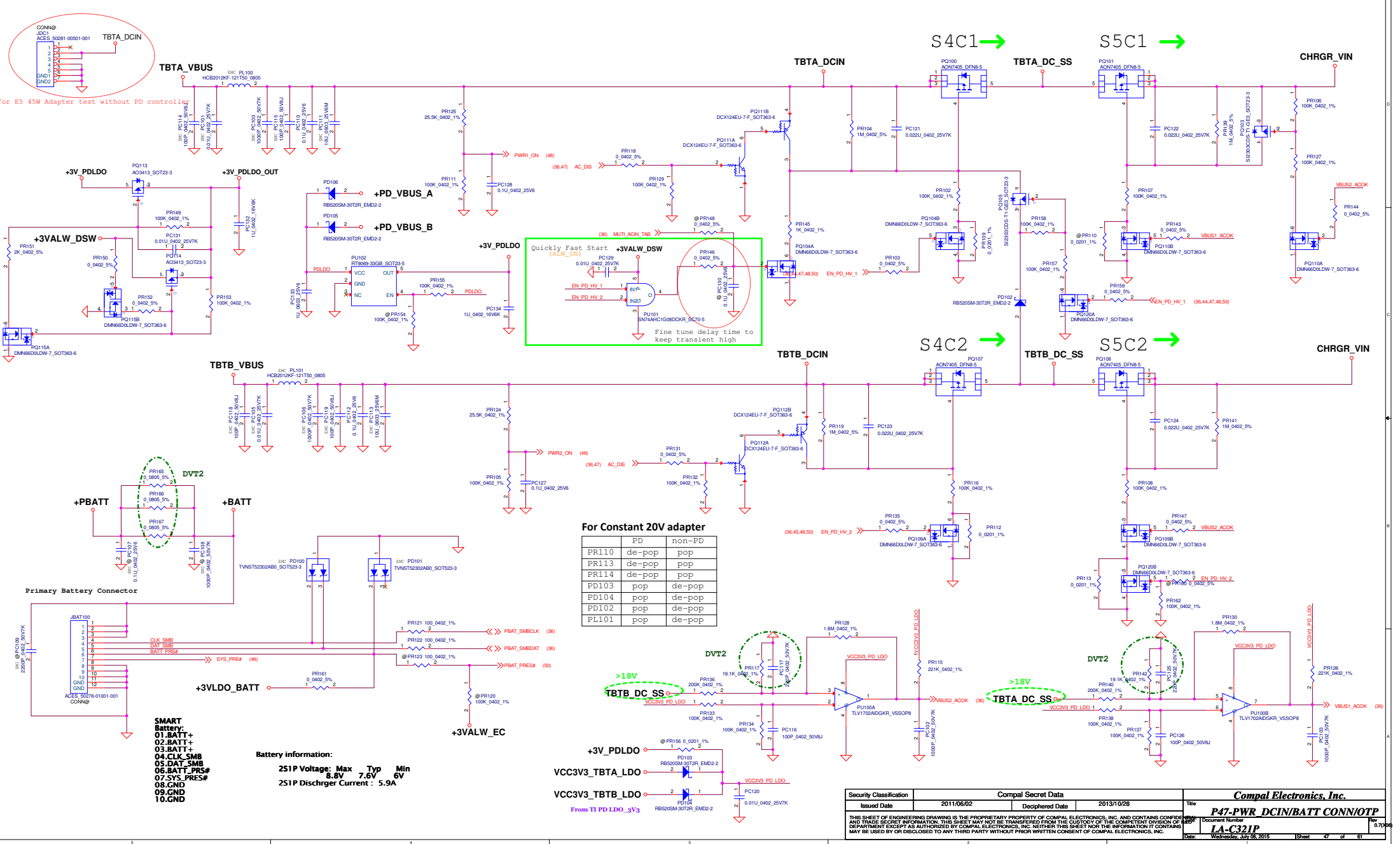


5	4	3	2	1																														
D				D																														
C				C																														
B				B																														
A				A																														
<div><table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td>Title</td></tr><tr><td>Issued Date</td><td>2014/09/08</td><td>Deciphered Date</td><td>2012/07/25</td><td>Compal Electronics, Inc.</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>P44-TBTA/B uController</td></tr><tr><td>Size</td><td colspan="3">Document Number</td><td>Rev</td></tr><tr><td>D</td><td colspan="3">LA-C321P</td><td>0.7(06)</td></tr><tr><td>Date:</td><td>Wednesday, July 08, 2015</td><td>Sheet</td><td>43</td><td>of 61</td></tr></table></div>					Security Classification	Compal Secret Data			Title	Issued Date	2014/09/08	Deciphered Date	2012/07/25	Compal Electronics, Inc.	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				P44-TBTA/B uController	Size	Document Number			Rev	D	LA-C321P			0.7(06)	Date:	Wednesday, July 08, 2015	Sheet	43	of 61
Security Classification	Compal Secret Data			Title																														
Issued Date	2014/09/08	Deciphered Date	2012/07/25	Compal Electronics, Inc.																														
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Size	Document Number			Rev																														
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Date:	Wednesday, July 08, 2015	Sheet	43	of 61																														
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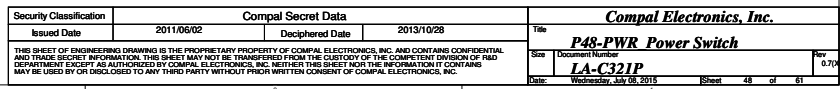


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						P47-TBT PORTA/B		
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						C	LA-C321P	0.70(06)
						Date:	Wednesday, July 08, 2015	Sheet






For Constant 20V adapter

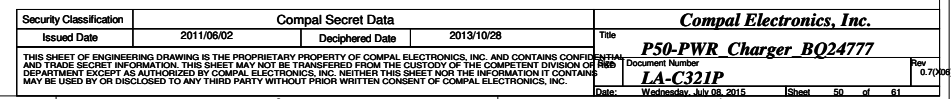
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PR110	de-pop	pop
PR113	de-pop	pop
PR114	de-pop	pop
PD103	pop	de-pop
PD104	pop	de-pop
PD102	pop	de-pop
PL101	pop	de-pop

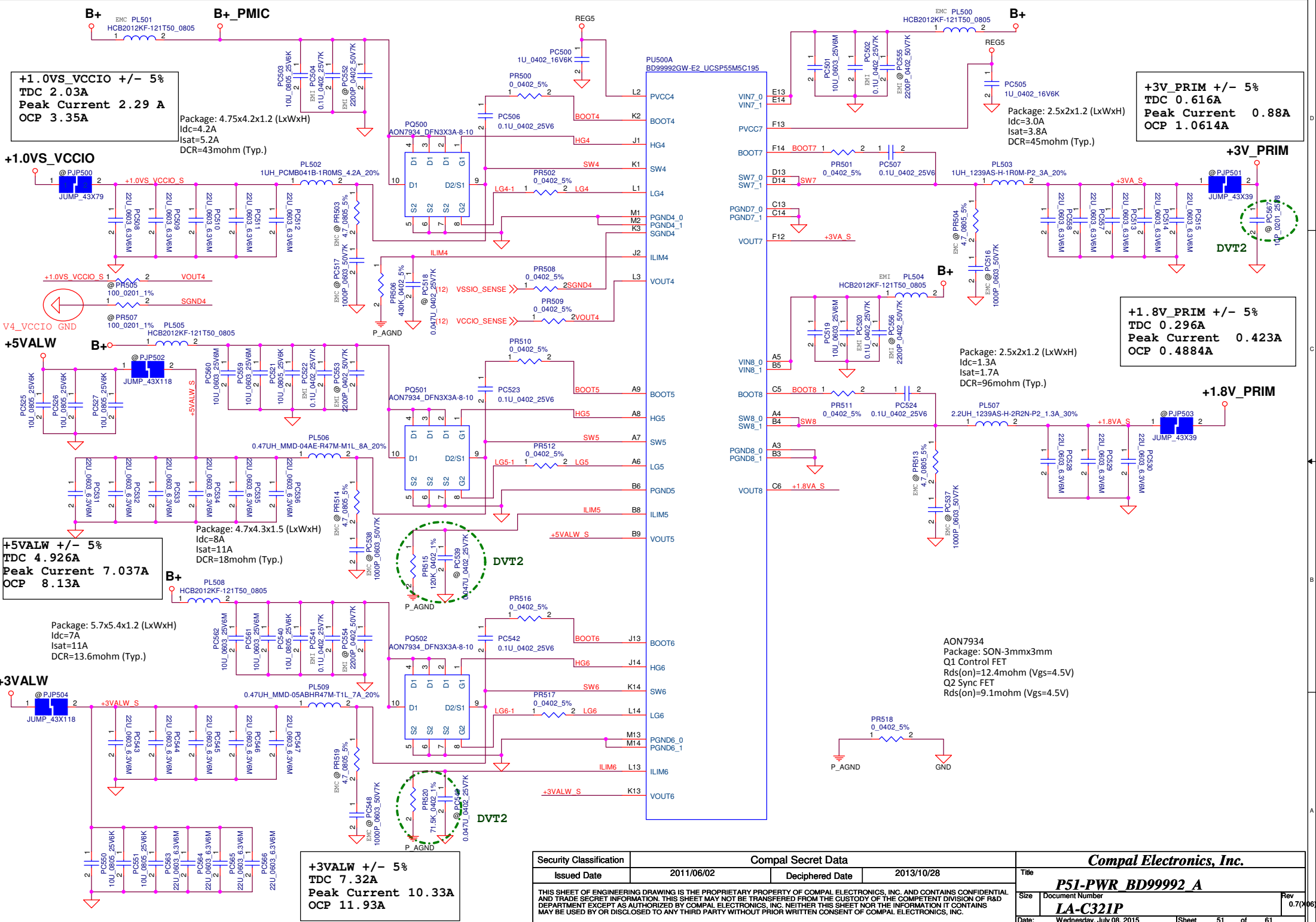




INPUTS			OUTPUTS Q
CLR	\bar{A}	B	
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	↑	
H	↓	H	
↑	L	H	

Security Classification		Compal Secret Data		Compal Electronics, Inc. P49-PWR BATT output 3.3V	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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					LA-C321P
				Rev	0.7(006)
				Date:	Wednesday, July 08, 2015
				Sheet	49 of 61





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P51-PWR BD99992 A
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				LA-C321P	
				Date	Wednesday, July 08, 2015
				Sheet	51 of 61

+1.8V_MEM +/- 5%
TDC 0.294A
Peak Current 0.42A
OCF 0.485A

+1.8V_MEM

+1.2V_VDDQ +/- 5%
TDC 3.78A
Peak Current 5.4A
OCF 6.237A

+1.2V_VDDQ

Package: 4.5x4x1.2 (LxWxH)
 Idc=6A
 Isat=6A
 DCR=19mohm (Typ.)

+1.0V_PRIM

+1.0V_PRIM +/- 5%
TDC 3.24A
Peak Current 3.29A
OCF 5.35A

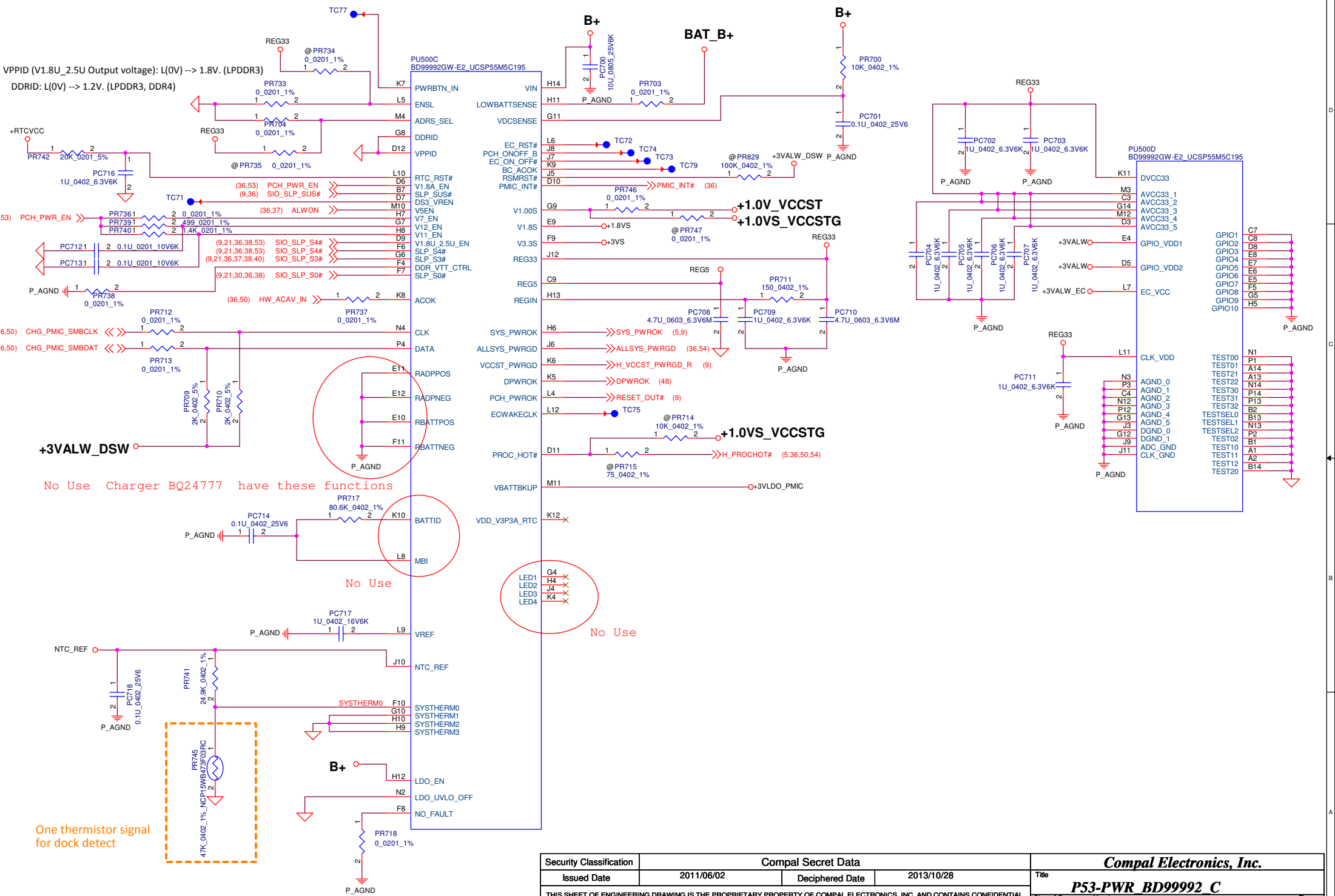
V0.85_PRIM +/- 5%
TDC 0.77A
Peak Current 1.1A
OCF 1.27A

+0.85V_PRIM

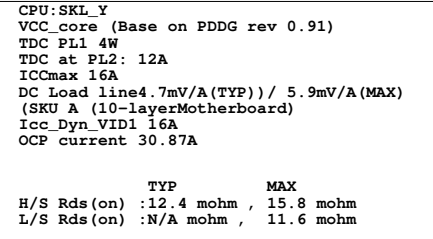
Package: 2.5x2x1.2 (LxWxH)
 Idc=1.3A
 Isat=1.7A
 DCR=96mohm (Typ.)

AON7934:
 Package: SON-3mmx3mm
 Q1 Control FET
 Rds(on)=12.4mohm (Vgs=4.5V)
 Q2 Sync FET
 Rds(on)=9.1mohm (Vgs=4.5V)

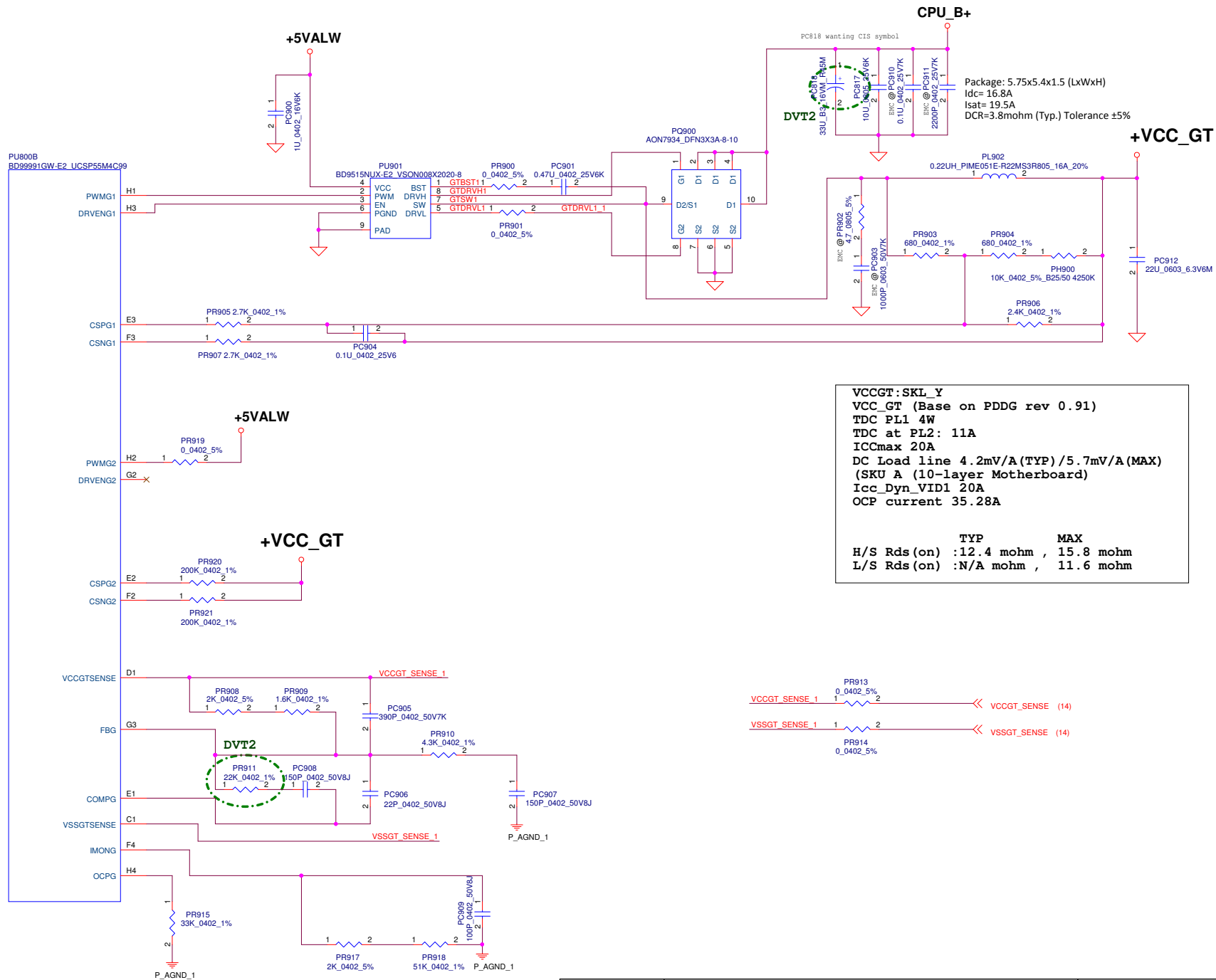
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P52-PWR BD99992_B
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				Date	Wednesday, July 08, 2015
				Sheet	52 of 61



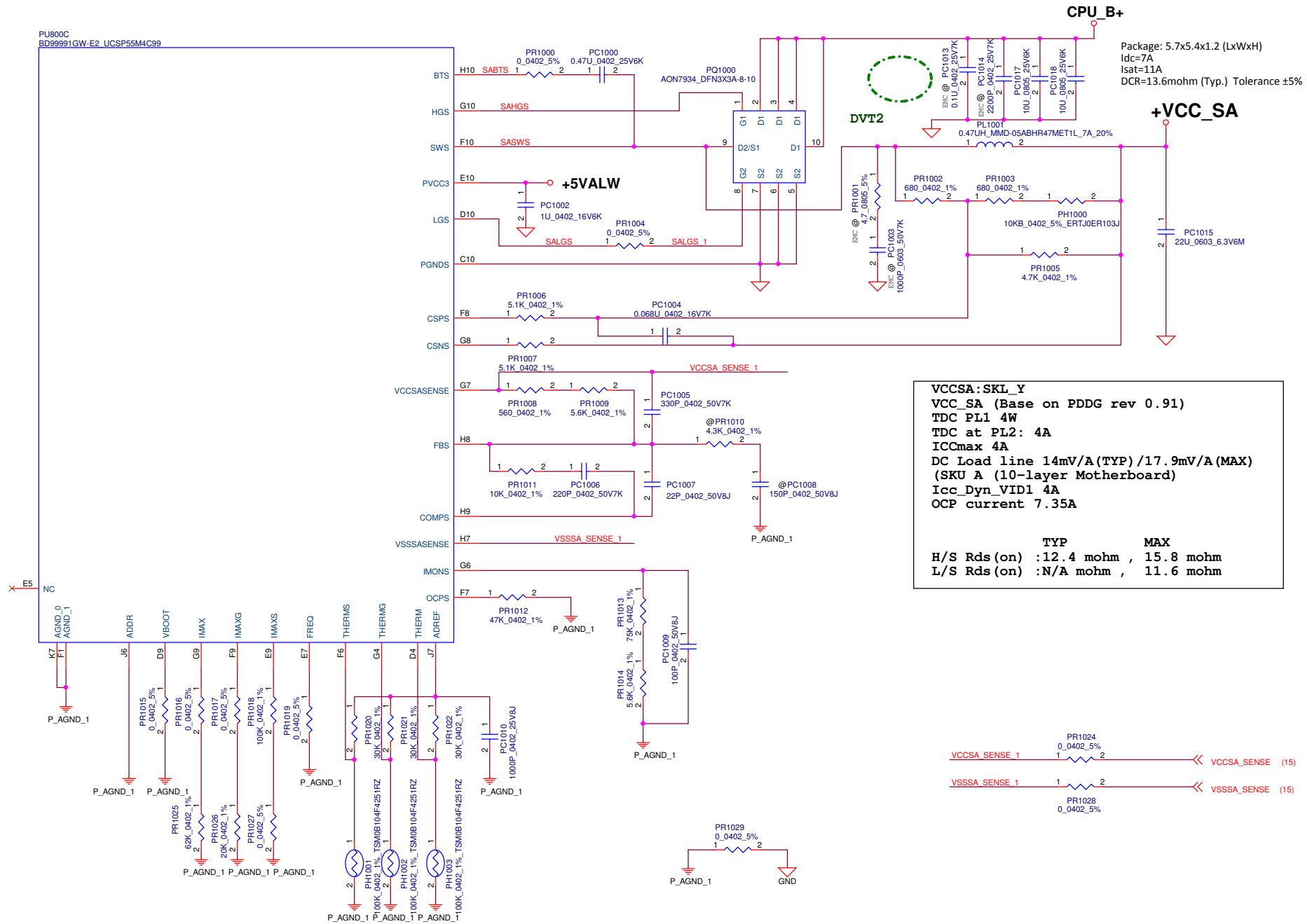
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P53-PWR BD99992 C
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				LA-C321P	Rev 0.7(006)
Date: Wednesday, July 08, 2015		Sheet 53 of 61			



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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P54-PWR BD99991 A
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				LA-C321P	
				Date:	Wednesday, July 06, 2015
				Sheet	54 of 61



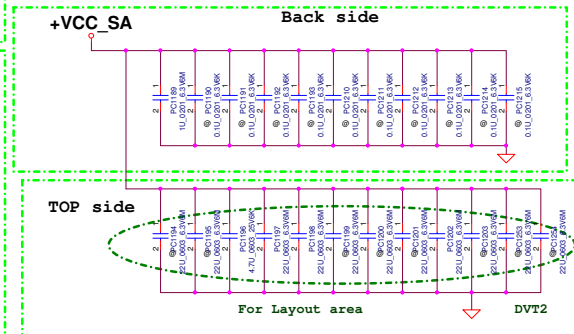
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P55-PWR BD99991 B
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				Date:	Wednesday, July 08, 2015
				Sheet	55 of 61



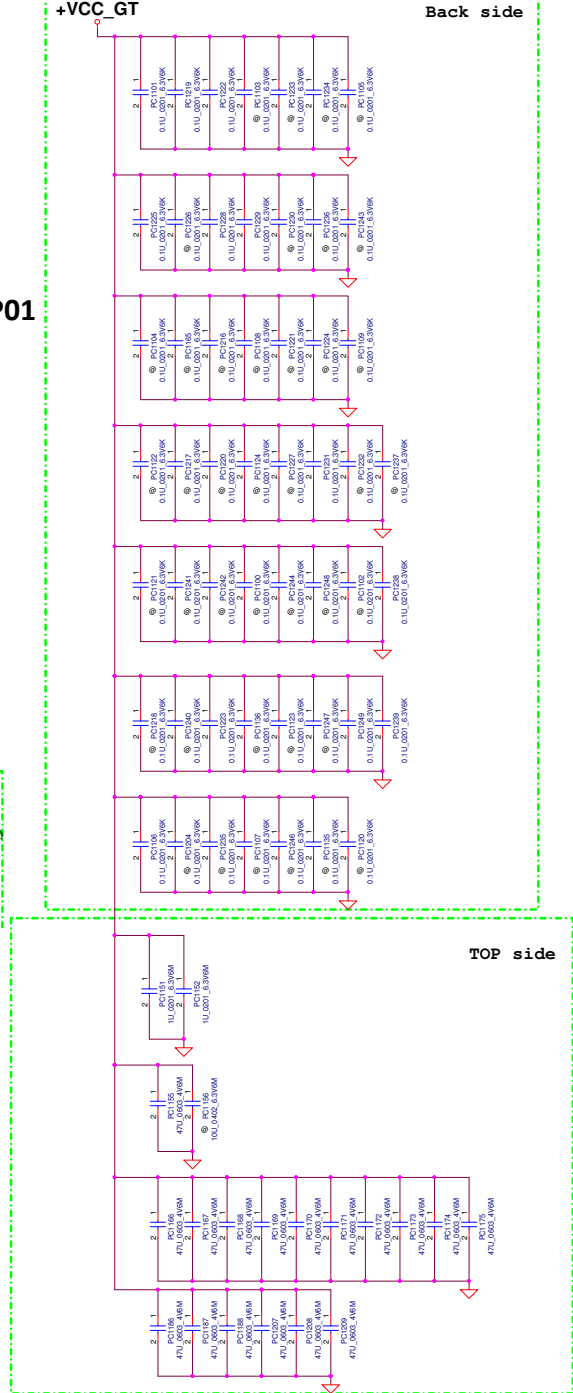
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				Date:	Wednesday, July 08, 2015
				Sheet	56 of 61

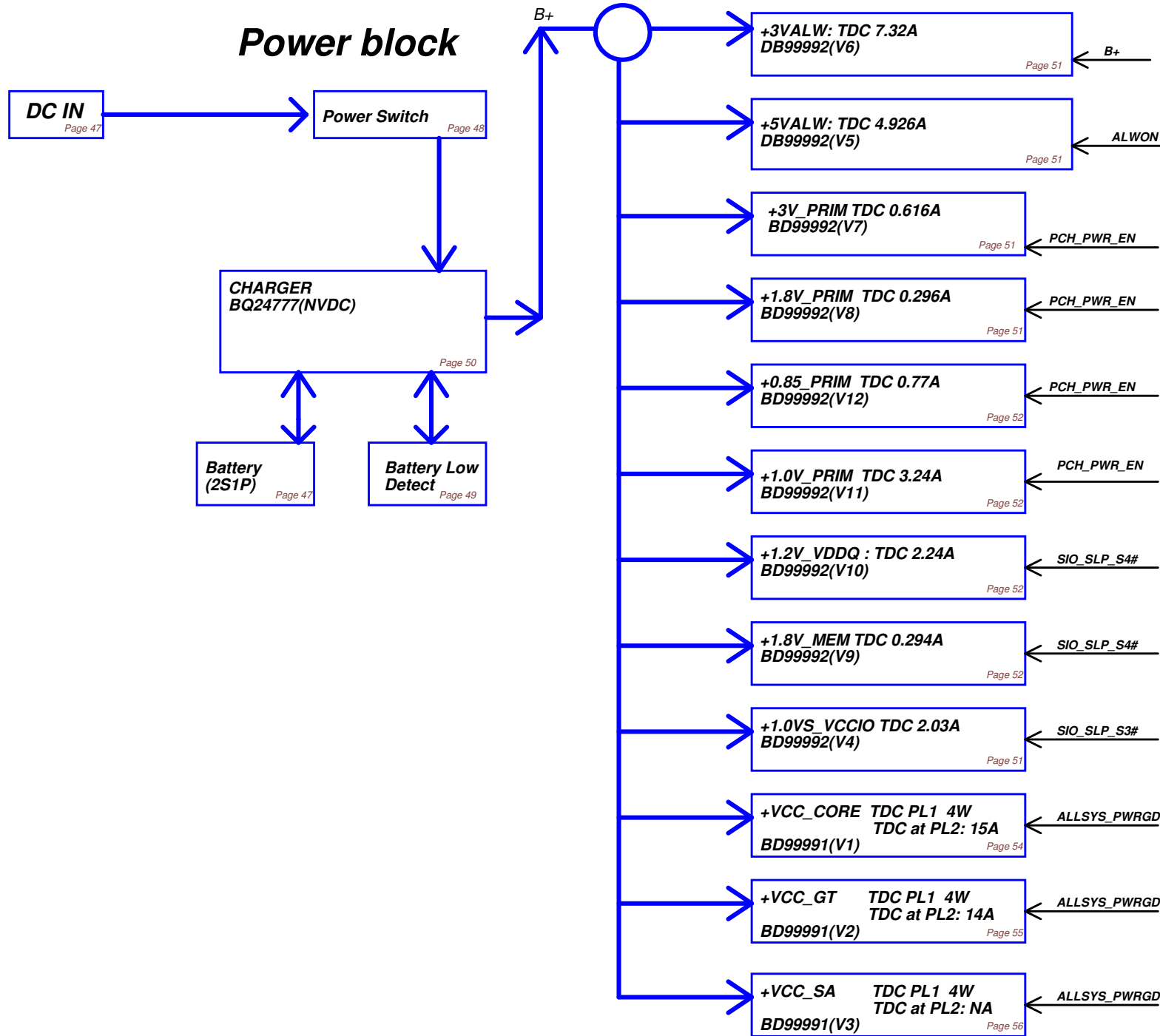
VCC_GT
0.1U_0201 * 12 pcs +1U_0201*2 pcs+47U_0603*16pcs+(Reserve 0.1U_0201*40pcs+10u_0402*2pcs)



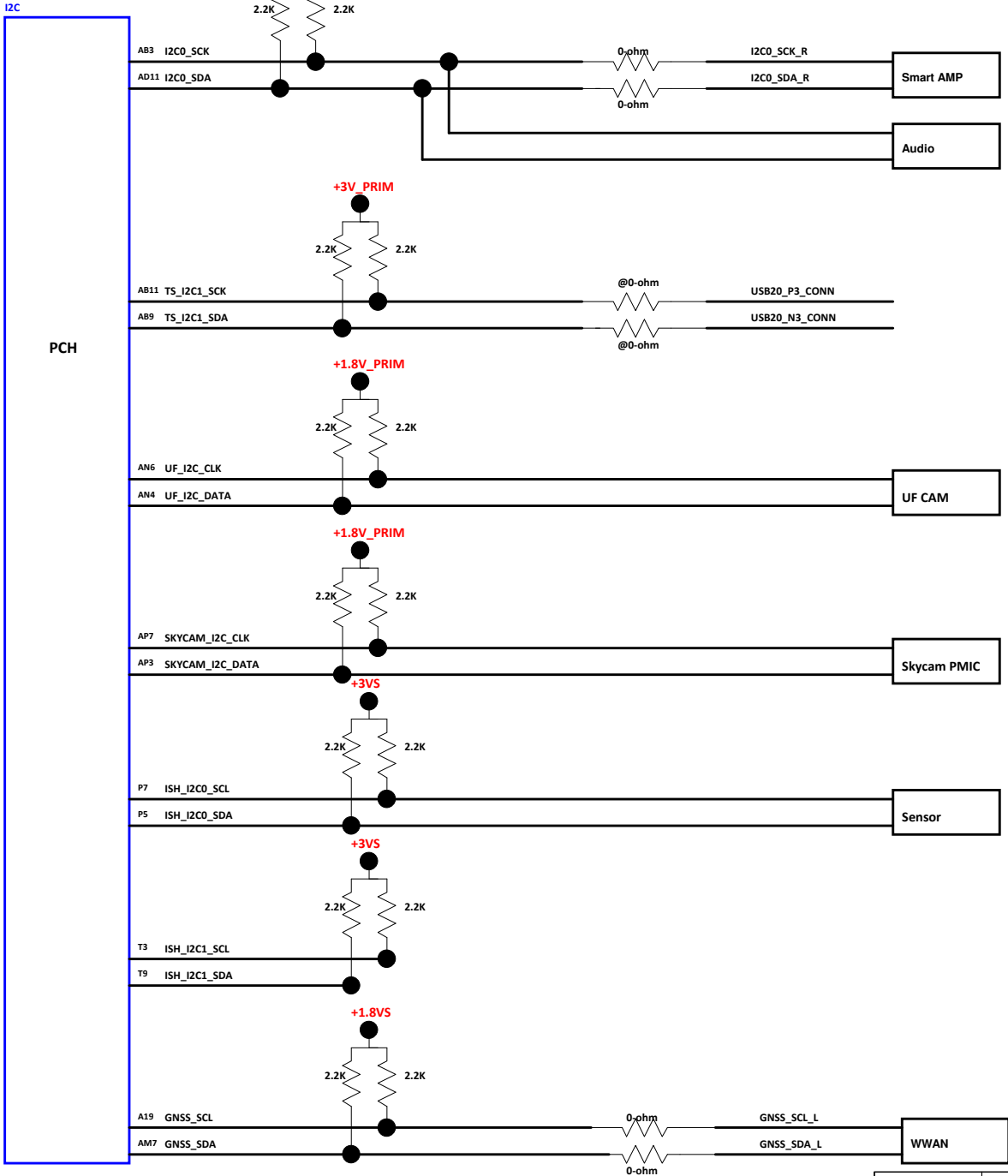
VCC_SA
1U_0201 * 1 pcs +22U_0603*8 pcs+(Reserve
0.1U_0201*10pcs+22u_0603*2pcs)



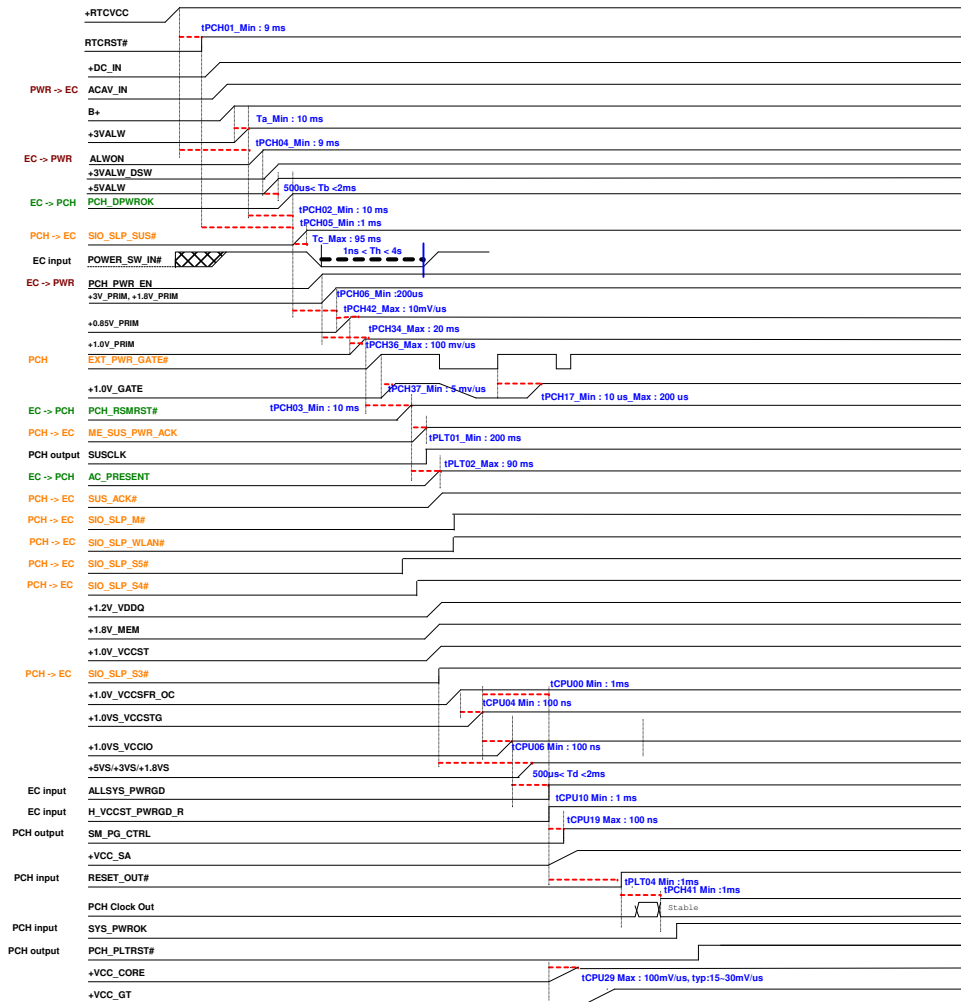
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/04/10	Deciphered Date	2014/05/01	Title	PWR POWER BLOCK DIAGRAM
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				Date	Wednesday, July 08, 2015
				Sheet	58 of 61
				Rev	0.70



[Power ON Sequence]



5					4					3					2					1				
D																								
C																								
B																								
A																								
5					4					3					2					1				
S																								

Security Classification		Compal Secret Data				Compal Electronics, Inc.									
Issued Date		2041/09/08		Deciphered Date		2012/07/25		Title							
								P63-Power Down Sequence							
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								Date:		Wednesday, July 08, 2015		Sheet 61 of 61		0.7/006	

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Issued Date		2041/09/08		Deciphered Date		2012/07/25		Title									
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								Size		Document Number						Rev	
								Date: Wednesday, July 08, 2015		Sheet		61		of		61	